Russia: LLC “ID Solution”, +7 495 545 3283,
www.idsolution.ru

EmETX-a58M1

AMD G-series Processor G-Series
ETX CPU Module

User’s Manual

Version 1.0

2017.04

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Table of Contents

Chapter 1 - Introduction 1
1.1 Copyright Notice 2
1.2 Declaration of Conformity 2
1.3 About This User’s Manual 4
1.4 Warning 4
1.5 Replacing the Lithium Battery 4
1.6 Technical Support 4
1.7 Warranty 5
1.8 Packing List 6
1.9 Ordering Information 6
1.10 Specifications 7
1.11 Board Dimensions 8
1.12 Board Layout Top View 9
1.13 Board Layout Bottom View 9
Chapter 2 - Installation 11
2.1 Connectors 12
2.2 Block Diagram 15
2.3 Driver Installation Paths 16
Chapter 3 - BIOS 17
3.1 Main 18
3.2 Advanced 20
3.2.1 ACPI Settings 21
3.2.2 CPU Configuraion 22
3.2.3 IDE Configuration 23
3.2.4 SDIO Configuration 24
3.2.5 USB Configuration 25
3.2.6 Super IO Configuration 26
3.2.7 H/W Monitor 27
3.2.8 Network Stack Configuration 28
3.3 Chipset 29
3.3.1 South Bridge 30
3.3.2 North Bridge 32
3.3.3 North Bridge LVDS Config Select 33

3.4 Boot 34
3.5 Security 36
3.6 Save & Exit 37
3.7 AMI BIOS Checkpoints 39
3.7.1 Checkpoint Ranges 39
3.7.2 Standard Checkpoints 40
Appendix 49
Appendix A: I/O Port Address Map 50
Appendix B: BIOS Memory Map 53
Appendix C: Interrupt Request Lines (IRQ) 54
Appendix D: Watchdog Timer (WDT) Setting 56

Chapter 1

Introduction

1.1 Copyright Notice

All Rights Reserved.

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

1.2 Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

> Warning
>
> This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union’s Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

1.3 About This User’s Manual

This user’s manual provides general information and installation instructions about the product. This User’s Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. please consult your vendor before further handling.

1.4 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

1.5 Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

1.6 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor-technology.com.tw

E-mail:info@arbor.com.tw

1.7 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product’s manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.8 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

1 x EmETX-a58M1 ETX® CPU Module

1 x Driver CD

1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

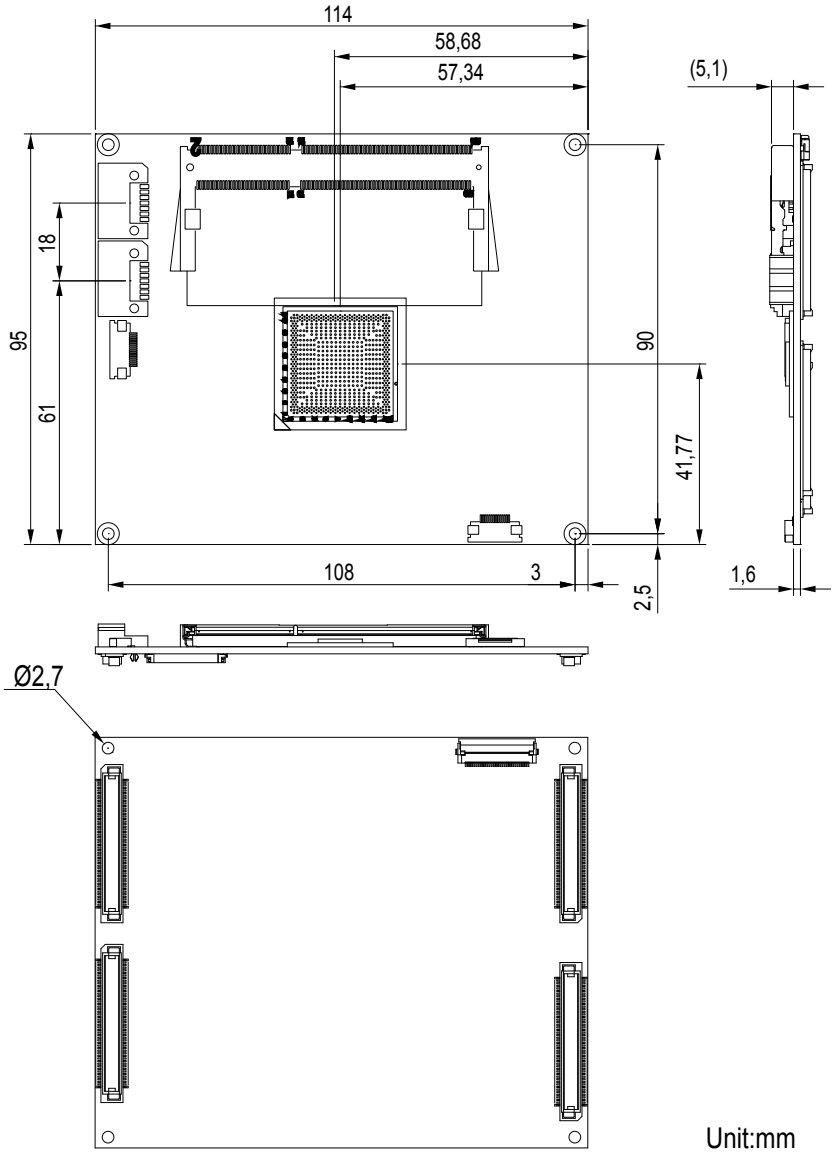
1.9 Ordering Information

EmETX-a58M1-212JC	AMD GX-212JC ETX 3.02 CPU module
EmETX-a58M1-218GL	AMD GX-218GL ETX 3.02 CPU module
HS-58M1-F2	Heat Spreader, Threaded standoffs,114*95*9mm,W/PAD
HS-58M1-C1	Heat Spreader, 114*95*28mm,W/FAN
PBE-1000 R2.1	ETX® evaluation board in ATX form factor
CBK-05-1000-00	Cable kit 1 x FDD cable 3 x COM port cables 1 x USB cable 2 x IDE cables 1 x TV-out cable

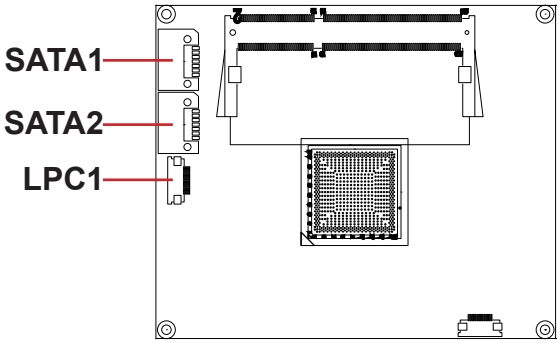
1.10 Specifications

Form Factor	ETX® CPU Module
CPU	Soldered onboard AMD G-Series Processor GX-212JC/GX-218GL
System Memory	1 x DDR3 SO-DIMM socket, supporting up to 8GB 1333MT/s SDRAM
BIOS	AMI BIOS
Watchdog Timer	1~255 level Reset
Super IO Chipset	Fintek F71869ED
Serial Port	2 x COM Ports (1 x RS-232, 1 x RS-232/422/485 selectable via PBE-1000)
Parallel Port	1 x SPP/EPP/ECP mode
KB/MS	Support PS/2 interface Keyboard and Mouse
USB 2.0	4 x USB 2.0 ports
Expansion	4 x PCI (OEM Request)
Storage	2 x Serial ATA ports with 600MB/s HDD transfer rate
	Two PATA ports via JMB368 PCIe to PATA controllers
Ethernet Chipset	1 x Realtek RTL8105E PCIe 10/100Base-T Ethernet controller
Audio	Realtek ALC662 HD Audio CODEC, Mic-in/ Line-in/ Line-out
Graphic Chipset	Integrated in AMD Radeon™ HD 8000E Graphics
Graphic Interface	Analog RGB/DVI: Analog RGB, with resolution up to LCD: Dual Channels 24-bit LVDS DDI port: 1 x DDI port
Power Requirement	DC 5V, 5VSB
Power Consumption	2.66A@5V(GX-212JC typical)
Operation Temp.	0 ~ 60ºC (0 ~ 140ºF)
Operating Humidity	0 ~ 95% @ 60ºC (non-condensing)
Dimension (L x W)	114 x 95 mm (4.5" x 3.7")

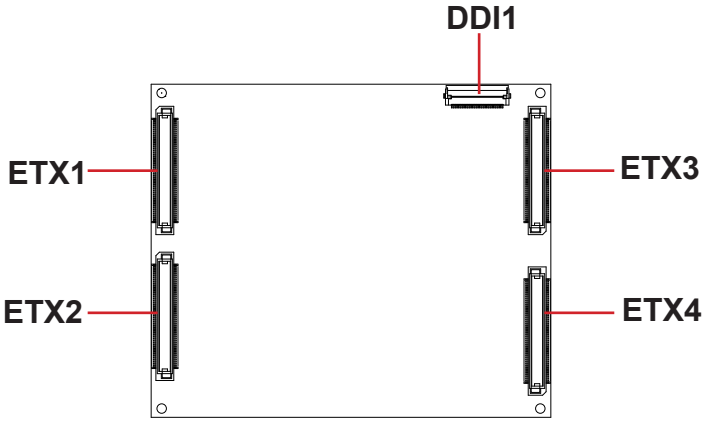
1.11 Board Dimensions



1.12 Board Layout Top View



1.13 Board Layout Bottom View



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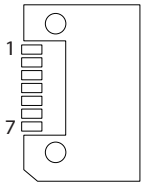
Chapter 2
Installation

2.1 Connectors

SATA1, SATA2 Connectors

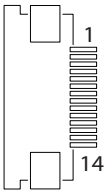
Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



LPC1 Connector

Connector type: FPC12-14P-P0.5 (Hirose)

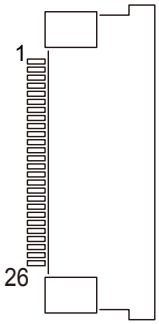
Pin	Description	Pin	Description
1	LAD0	8	BUF_PLT_RST#
2	LAD1	9	GND
3	LAD2	10	PCLK_CONN
4	LAD3	11	GND
5	GND	12	GND
6	LFRAME#	13	+3.3V
7	INT_SERIRQ	14	+3.3V



DDI1 Connector

Connector type: FH12-26S-0.5SH (Hirose)

Pin	Description	Pin	Description
1	GND	14	N/C
2	DDI_TX0+	15	DDI_AUX+
3	DDI_TX0-	16	DDI_AUX-
4	GND	17	GND
5	DDI_TX1+	18	DDI_HPD
6	DDI_TX1-	19	SMB_DAT
7	GND	20	SMB_CLK
8	DDI_TX2+	21	GND
9	DDI_TX2-	22	GND
10	GND	23	GND
11	DDI_TX3+	24	+3.3V
12	DDI_TX3-	25	+3.3V
13	GND	26	+5V



ETX1 Connector

A1	GND	GND	A2
A3	PCI_CLK3	PCI_CLK4	A4
A5	GND	GND	A6
A7	PCI_CLK1	PCI_CLK2	A8
A9	REQ#3	GNT#3	A10
A11	GNT#2	VCC3	A12
A13	REQ#2	GNT#1	A14
A15	REQ#1	VCC3	A16
A17	GNT#0	N.C	A18
A19	VCC	VCC	A20
A21	SERIRQ	REQ#0	A22
A23	AD0	VCC3	A24
A25	AD1	AD2	A26
A27	AD4	AD3	A28
A29	AD6	AD5	A30
A31	C/BE#0	AD7	A32
A33	AD8	AD9	A34
A35	GND	GND	A36
A37	AD10	LINE-L	A38
A39	AD11	MICL	A40
A41	AD12	LINE-R	A42
A43	AD13	ASVCC	A44
A45	AD14	LOUT-L	A46
A47	AD15	ASGND	A48
A49	C/BE#1	LOUT-R	A50
A51	VCC	VCC	A52
A53	PAR	SERR#	A54
A55	PERR#	N.C	A56
A57	PME#	USB8N	A58
A59	LOCK#	DEVSEL#	A60
A61	TRDY#	USB9N	A62
A63	IRDY#	STOP#	A64
A65	FRAME#	USB8P	A66
A67	GND	GND	A68
A69	AD16	CBE#2	A70
A71	AD17	USB9P	A72
A73	AD19	AD18	A74
A75	AD20	USB0N	A76
A77	AD22	AD21	A78
A79	AD23	USB1N	A80
A81	AD24	C/BE#3	A82
A83	VCC	VCC	A84
A85	AD25	AD26	A86
A87	AD28	USB0P	A88
A89	AD27	AD29	A90
A91	AD30	USB1P	A92
A93	PCI_RST#	AD31	A94
A95	INT_PIRQB#	INT_PIRQC#	A96
A97	INT_PIRQD#	INT_PIRQA#	A98
A99	GND	GND	A100

ETX2 Connector

B1	GND	GND	B2
B3	N.C	N.C	B4
B5	N.C	N.C	B6
B7	N.C	N.C	B8
B9	N.C	N.C	B10
B11	N.C	N.C	B12
B13	N.C	N.C	B14
B15	N.C	N.C	B16
B17	N.C	N.C	B18
B19	N.C	N.C	B20
B21	N.C	N.C	B22
B23	N.C	N.C	B24
B25	N.C	N.C	B26
B27	N.C	N.C	B28
B29	N.C	N.C	B30
B31	N.C	N.C	B32
B33	N.C	N.C	B34
B35	GND	GND	B36
B37	N.C	N.C	B38
B39	N.C	N.C	B40
B41	N.C	N.C	B42
B43	N.C	TC	B44
B45	N.C	N.C	B46
B47	N.C	N.C	B48
B49	N.C	N.C	B50
B51	VCC	VCC	B52
B53	N.C	N.C	B54
B55	N.C	N.C	B56
B57	N.C	N.C	B58
B59	N.C	N.C	B60
B61	N.C	N.C	B62
B63	N.C	N.C	B64
B65	N.C	N.C	B66
B67	GND	GND	B68
B69	N.C	N.C	B70
B71	N.C	N.C	B72
B73	N.C	N.C	B74
B75	N.C	N.C	B76
B77	N.C	N.C	B78
B79	N.C	N.C	B80
B81	N.C	N.C	B82
B83	VCC	VCC	B84
B85	N.C	N.C	B86
B87	N.C	N.C	B88
B89	N.C	N.C	B90
B91	N.C	N.C	B92
B93	N.C	N.C	B94
B95	N.C	N.C	B96
B97	N.C	N.C	B98
B99	GND	GND	B100

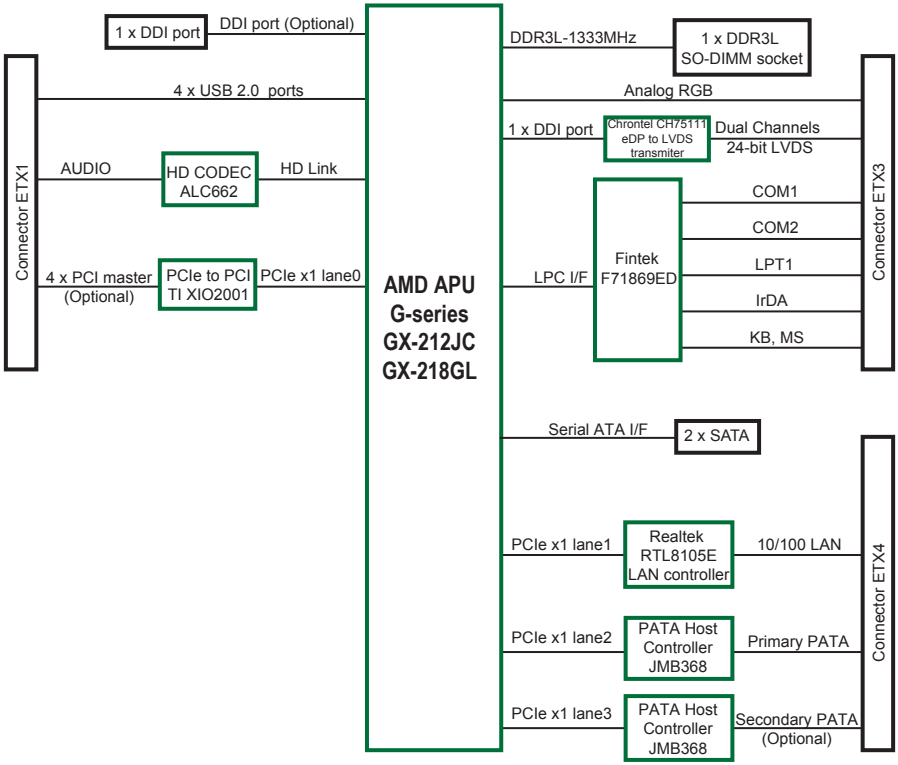
ETX3 Connector

C1	GND	GND	C2
C3	CRT_RED	CRT_BLUE	C4
C5	HSY	CRT_GREEN	C6
C7	VSY	CRT_DDC_CLK	C8
C9	N.C	CRT_DDC_DATA	C10
C11	LVDS_B_CLK-	LVDS_B3-	C12
C13	LVDS_B_CLK+	LVDS_B3+	C14
C15	GND	GND	C16
C17	LVDS_B1+	LVDS_B2+	C18
C19	LVDS_B1-	LVDS_B2-	C20
C21	GND	GND	C22
C23	LVDS_A3-	LVDS_B0+	C24
C25	LVDS_A3+	LVDS_B0-	C26
C27	GND	GND	C28
C29	LVDS_A2-	LVDS_A_CLK+	C30
C31	LVDS_A2+	LVDS_A_CLK-	C32
C33	GND	GND	C34
C35	LVDS_A0+	LVDS_A1+	C36
C37	LVDS_A0-	LVDS_A1-	C38
C39	VCC	VCC	C40
C41	LVDS_I2C_DAT	N.C.	C42
C43	LVDS_I2C_CLK	LVDS_-BLON	C44
C45	LVDS_BKLT_CTRL	LVDS_ENVDD	C46
C47	N.C.	N.C.	C48
C49	N.C.	N.C.	C50
C51	LPT_FLPY#	N.C.	C52
C53	VCC	GND	C54
C55	STB#	AFD#	C56
C57	N.C.	PD7	C58
C59	IRRX	ERR#	C60
C61	IRTX	PD6	C62
C63	SIN2	INIT#	C64
C65	GND	GND	C66
C67	RTS2#	PD5	C68
C69	DTR2#	SLIN#	C70
C71	DCD2#	PD4	C72
C73	DSR2#	PD3	C74
C75	CTS2#	PD2	C76
C77	SOUT2	PD1	C78
C79	RI2#	PD0	C80
C81	VCC	VCC	C82
C83	SIN1	ACK#	C84
C85	RTS1#	BUSY	C86
C87	DTR1#	PE	C88
C89	DCD1#	SLCT	C90
C91	DSR1#	MCLK	C92
C93	CTS1#	MDAT	C94
C95	SOUT1	KCLK	C96
C97	RI1#	KDAT	C98
C99	GND	GND	C100

ETX4 Connector

D1	GND	GND	D2
D3	5V_SB	ETX_PWGIN	D4
D5	PSON#	ETX_SPEAK_OUT	D6
D7	CB_PWR_BTN#	+V3.3A_RTC	D8
D9	N.C	LILED1	D10
D11	WDTRST#	ACTLED1	D12
D13	N.C	SPLED1	D14
D15	N.C	I2C0_CLK	D16
D17	VCC	VCC	D18
D19	USB_-OC	N.C	D20
D21	EXSMI	I2C0_DAT	D22
D23	SCLK0	SDATA0	D24
D25	IDE_SDCS3-	SMB_ALERT#	D26
D27	IDE_SDCS1-	N.C	D28
D29	IDE_SDA2	IDE_PDCS3-	D30
D31	IDE_SDA0	IDE_PDCS1-	D32
D33	GND	GND	D34
D35	PDIAG_S	IDE_PDA2	D36
D37	IDE_SDA1	IDE_PDA0	D38
D39	IDE_SDDINTRQ	IDE_PDA1	D40
D41	-BATLOW	N.C	D42
D43	IDE_SDDACK-	IDE_PDDINTRQ	D44
D45	IDE_SDIORDY	IDE_PDDACK-	D46
D47	IDE_SDIOR-	IDE_PDIORDY	D48
D49	VCC	VCC	D50
D51	IDE_SDIOW-	IDE_PDIOR-	D52
D53	IDE_SDDREQ	IDE_PDIOW-	D54
D55	IDE_SDD15	IDE_PDDREQ	D56
D57	IDE_SDD0	IDE_PDD15	D58
D59	IDE_SDD14	IDE_PDD0	D60
D61	IDE_SDD1	IDE_PDD14	D62
D63	IDE_SDD13	IDE_PDD1	D64
D65	GND	GND	D66
D67	IDE_D2	IDE_PDD13	D68
D69	IDE_D12	IDE_PDD2	D70
D71	IDE_D3	IDE_PDD12	D72
D73	IDE_D11	IDE_PDD3	D74
D75	IDE_D4	IDE_PDD11	D76
D77	IDE_D10	IDE_PDD4	D78
D79	IDE_D5	IDE_PDD10	D80
D81	VCC	VCC	D82
D83	IDE_D9	IDE_PDD5	D84
D85	IDE_D6	IDE_PDD9	D86
D87	IDE_D8	IDE_PDD6	D88
D89	LPC_PME#	IDE_CBLID_P	D90
D91	RDN0	IDE_PDD8	D92
D93	RDP0	IDE_SDD7	D94
D95	TDN0	IDE_PDD7	D96
D97	TDP0	IDE_RST#	D98
D99	GND	GND	D100

2.2 Block Diagram



2.3 Driver Installation Paths

Windows 7

Driver	Path
CHIPSET	\EmETX-58M1\Chipset\Win7_Win10\16.40.2802-161004a-308065C-AES
LAN	\EmETX-58M1\LAN\Install_Win7_7101_09212016
AUDIO	\EmETX-58M1\Audio

Windows 10

Driver	Path
CHIPSET	\EmETX-58M1\Chipset\Win7_Win10\16.40.2802-161004a-308065C-AES
LAN	\EmETX-58M1\LAN\Install_Win10_10010_09212016
AUDIO	\EmETX-58M1\Audio

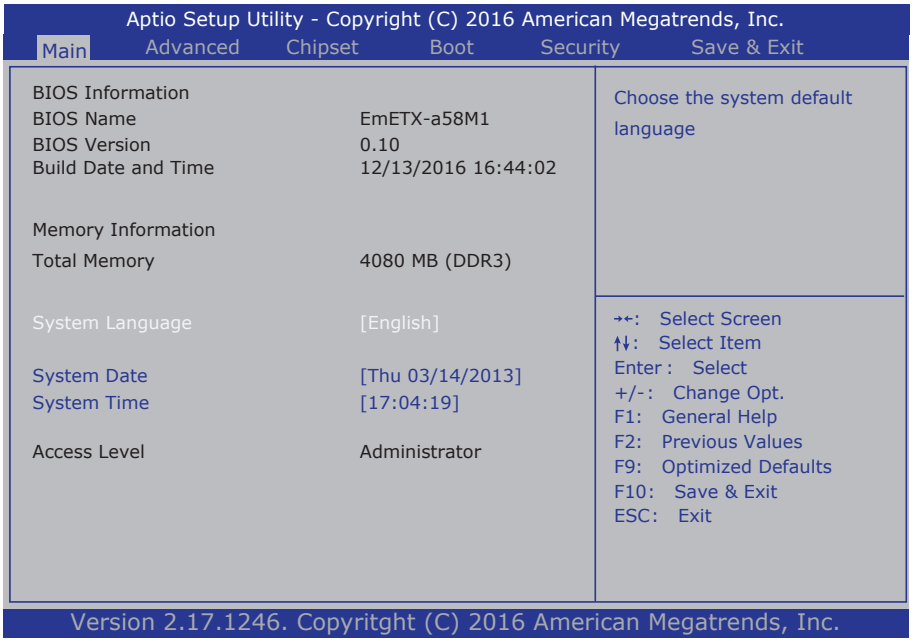
Chapter 3

BIOS

3.1 Main

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS RAM of the system stores the Setup utility and configurations. When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILITY, press **“Delete”** once the power is turned on. When the computer is shut down, the battery on the motherboard supplies the power for BIOS RAM.

The **Main Setup** screen lists the following information:



Item	Description
System Language	Choose the system default language
System Date	Set the system date. Use Tab to switch between Data elements. Note that the ‘Day’ automatically changes when you set the date. ► The date format is: **Day:** Sun to Sat **Month:** 1 to 12 **Date:** 1 to 31 **Year:** 1998 to 2099

System Time	Set the system time. Use Tab to switch between Time elements. ► The time format is: **Hour:** 00 to 23 **Minute:** 00 to 59 **Second:** 00 to 59

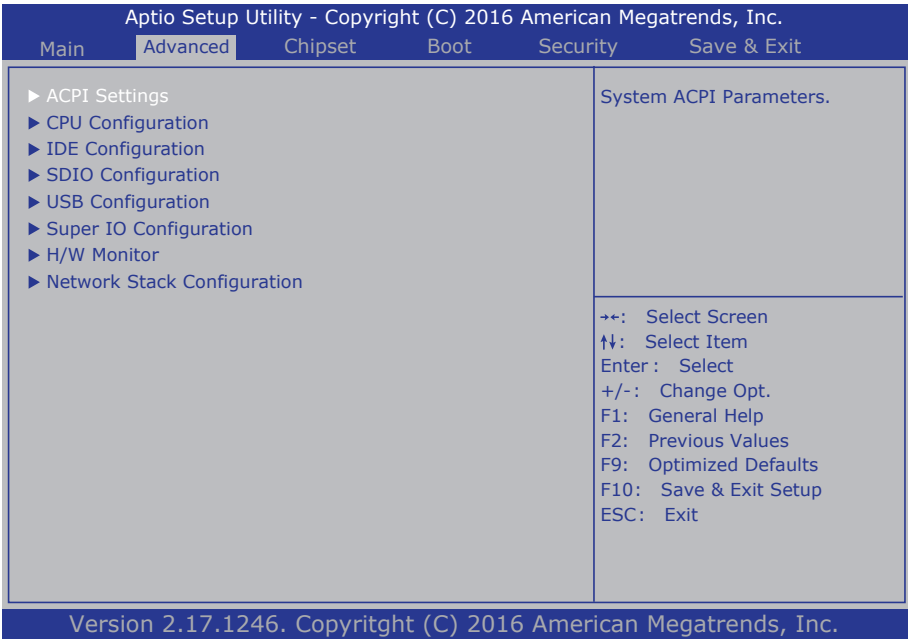
Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

Keystroke	Function
◄ ►	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
▼ ▲	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select “OK” or “Cancel” for exiting and discarding changes. Use “←” and “→” to select and press “Enter” to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down -	Decrease the numeric value on a selected setup item / make change
F1	Activate “General Help” screen
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select “OK” or “Cancel” for exiting and saving changes. Use “←” and “→” to select and press “Enter” to confirm)

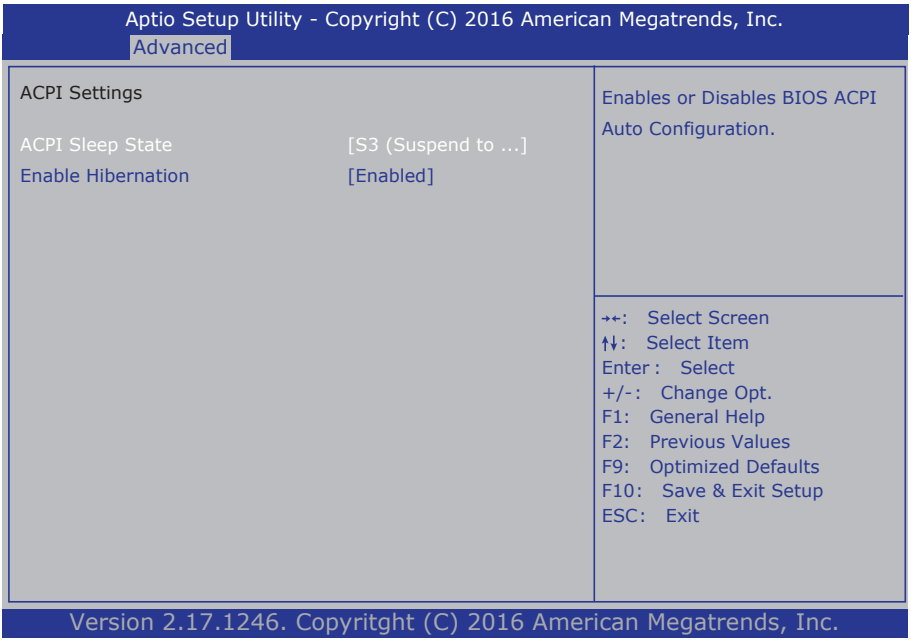
3.2 Advanced

The “Advanced” setting page provides you the options to configure the details of your hardware, such as PCI, ACPI, IDE, USB and Super IO.



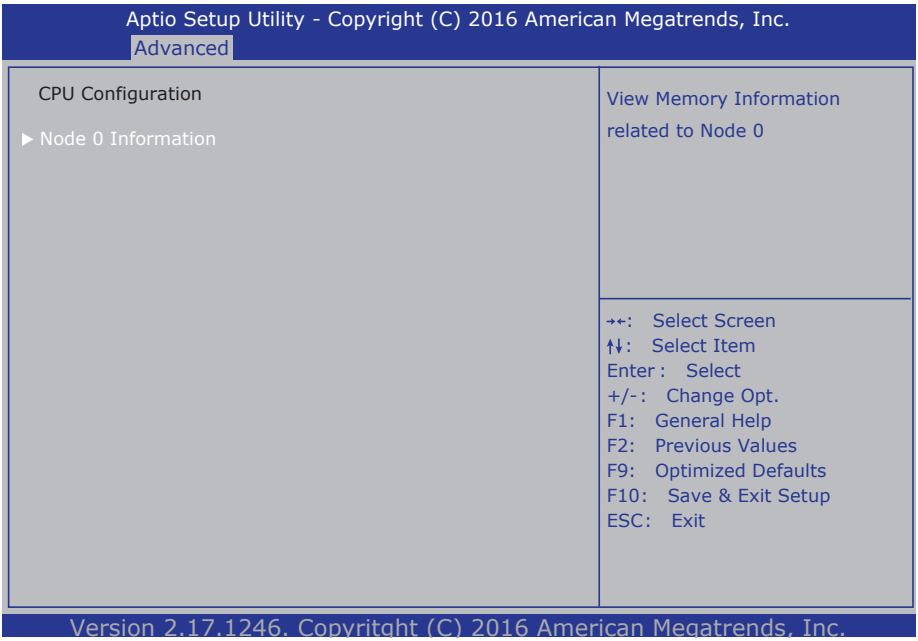
Item	Description
ACPI Configuration	3.2.1 ACPI Settings on page 21
CPU Configuration	3.2.2 CPU Configuraion on page 22
IDE Configuration	3.2.3 IDE Configuration on page 23
SDIO Configuration	3.2.4 SDIO Configuration on page 24
USB Configuration	3.2.5 USB Configuration on page 25
Super IO Configuration	3.2.6 Super IO Configuration on page 26
H/M Monitor	3.2.7 H/W Monitor on page 27
Network Stack Configuration	3.2.8 Network Stack Configuration on page 28

3.2.1 ACPI Settings



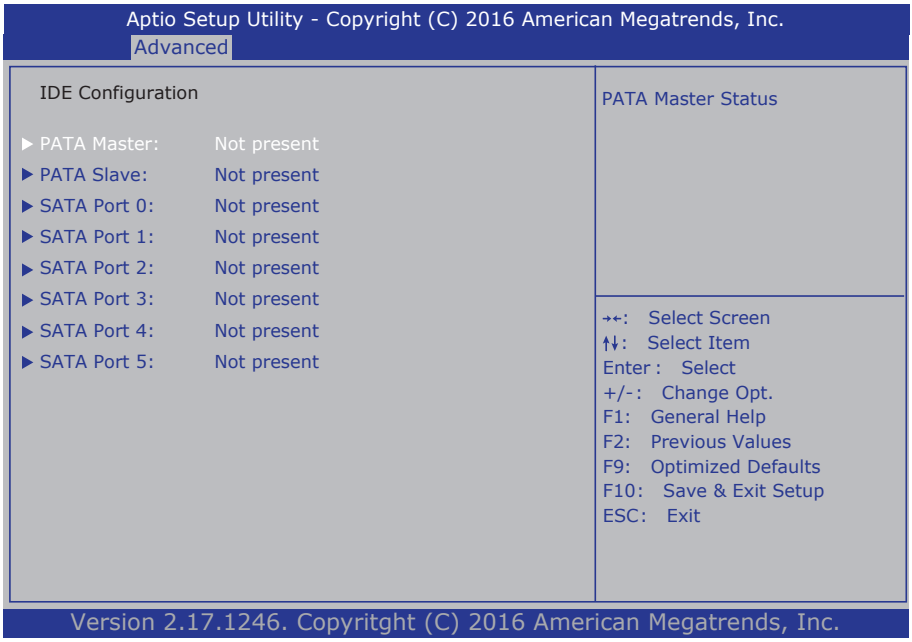
Item	Description
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed. ► Options: **Suspend Disabled**, **S1 only (CPU Stop Clock)**, **S3 (Suspend to RAM)** (default).
Enable Hibernation	**Enable** (default) or **Disable** system ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

3.2.2 CPU Configuraion



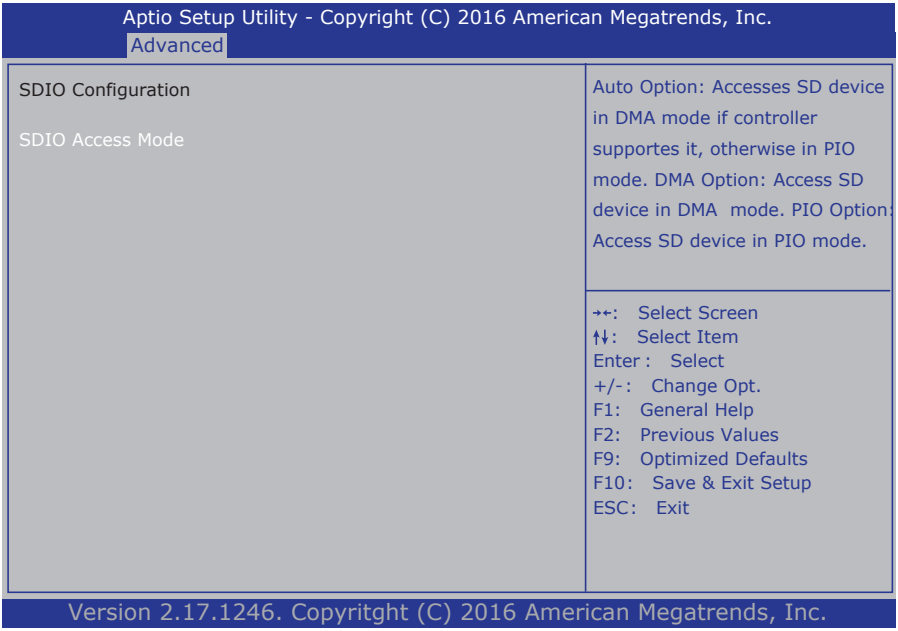
Item	Description
Node 0 Information	View Memory Information related to Node 0.

3.2.3 IDE Configuration



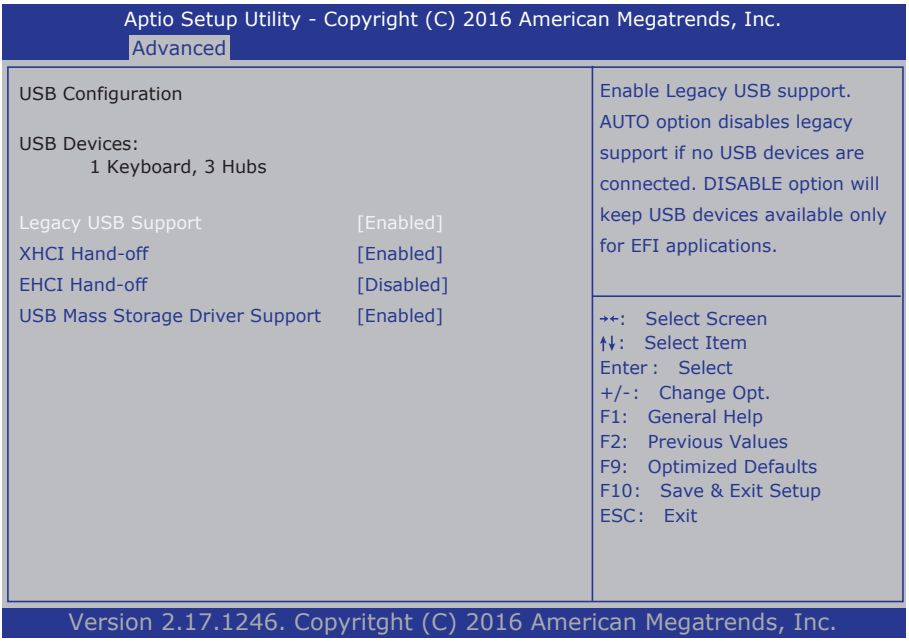
Item	Description
PATA Master/Slave SATA Port 0~5	Shows PATA Master/Slave and SATA ports information, if present.
PIO Mode	Programmed Input/Output Mode. ► Options: **Auto** (default), **00**, **01**, **02**, **03** and **04**.
DMA Mode	Direct Memory Access Mode. ► Options: **Auto** (default), **SWDMA0/1/2**, **MWDMA0/1/2** and **UDMA0/1/2/3/4/5/6**.

3.2.4 SDIO Configuration



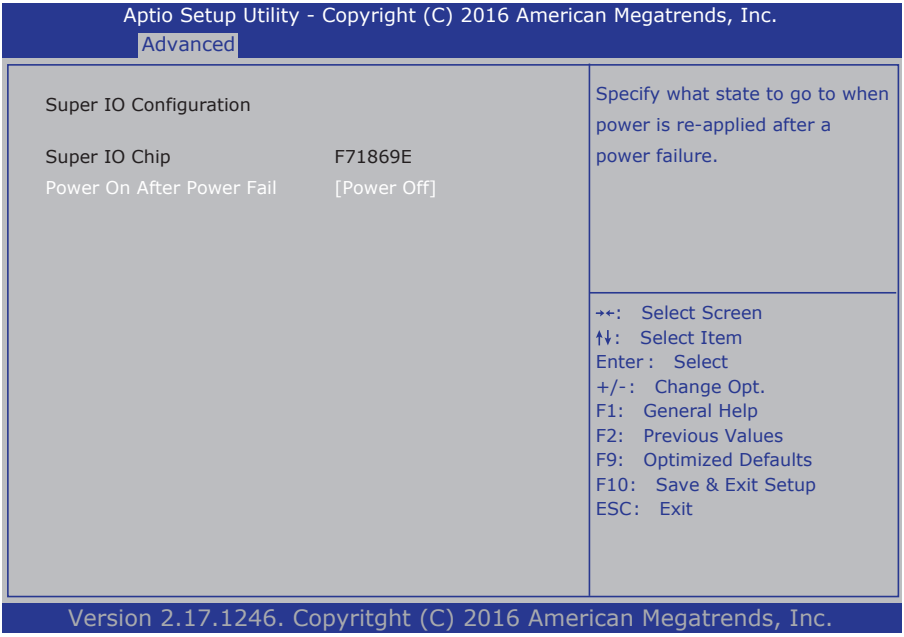
Item	Description
SDIO Access Mode	Set SDIO access mode. Options: ► **Auto** (default) **:** Accesses SD device in DMA mode if controller supportes it, otherwise in PIO mode. ► **DMA:** Access SD device in DMA mode. ► **PIO:** Access SD device in PIO mode.

3.2.5 USB Configuration



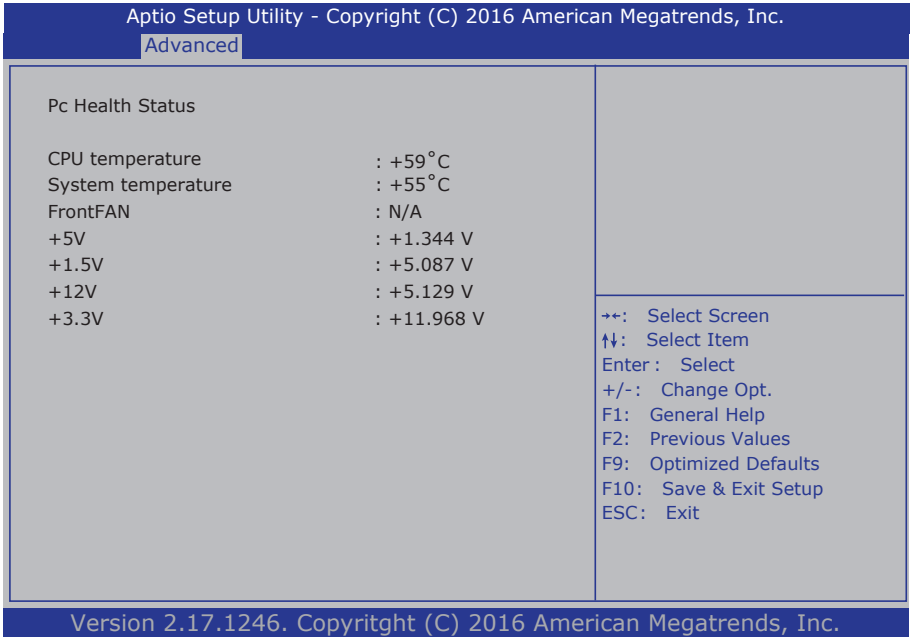
Item	Description
Legacy USB Support	**Enables** (default) Legacy USB support. **AUTO** option disables legacy support if no USB devices are connected. **DISABLE** option will keep USB devices available only for EFI applications.
XHCI Hand-off	Enables/disables a workaround for the operating systems that have no XHCI hand-off support ► Options: **Disabled** and **Enabled** (default)
EHCI Hand-off	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver. ► Options: **Disabled** (default) and **Enabled**
USB Mass Storage Driver Support	Enables/disables the support for USB mass storage driver. ► Options: **Disabled** and **Enabled** (default)

3.2.6 Super IO Configuration

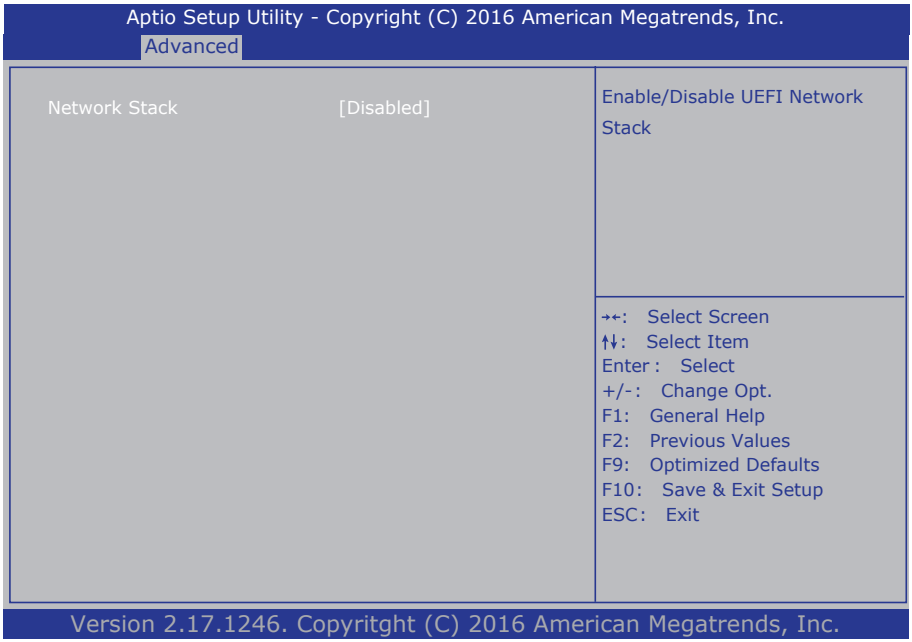


Item	Description
Power On After Power Fail	Specify what state to go to when power is re-applied after a power failure. ► Options: **Last State**, **Power On** and **Power off** (default)

3.2.7 H/W Monitor

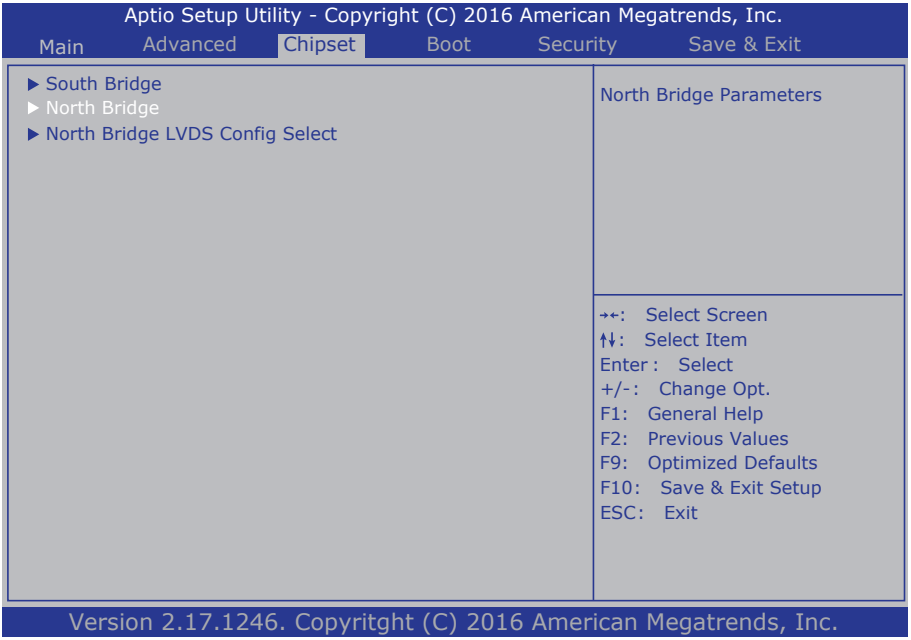


3.2.8 Network Stack Configuration



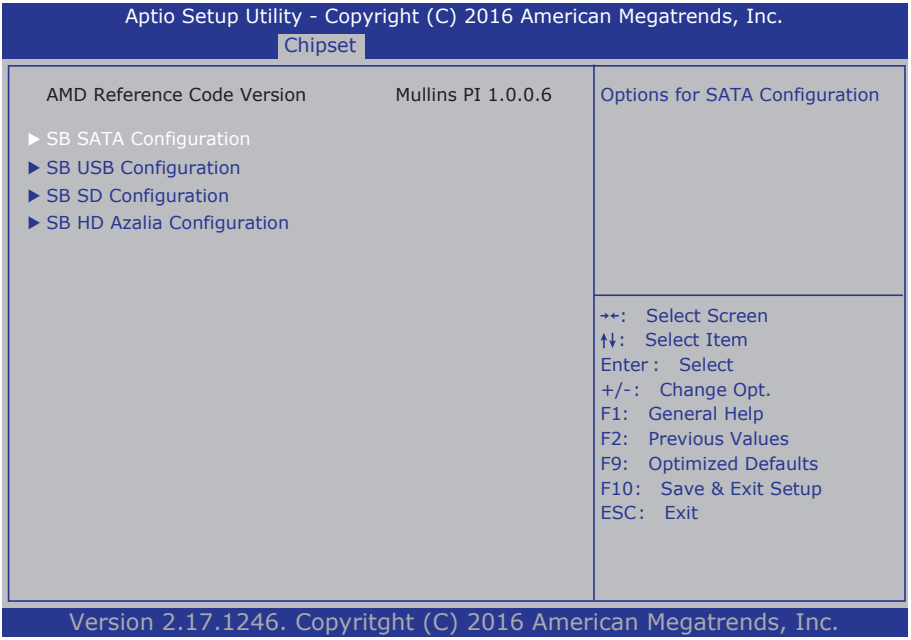
Item	Description
Network Stack	**Enable**/**Disable** (default) UEFI Network Stack

3.3 Chipset



Item	Description
North Bridge	3.3.2 North Bridge on page 32
North Bridge LVDS Config Select	3.3.3 North Bridge LVDS Config Select on page 33
South Bridge	3.3.1 South Bridge on page 30

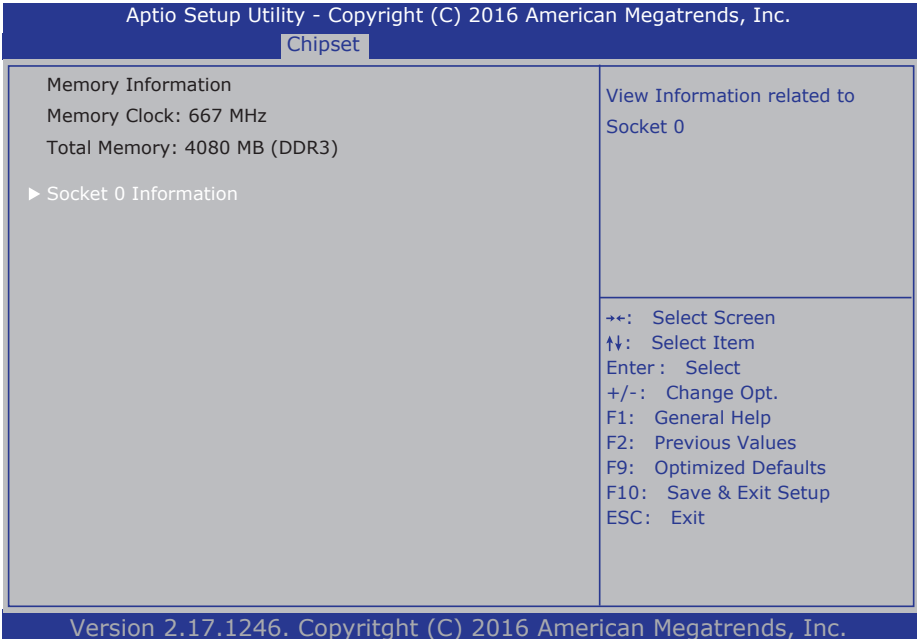
3.3.1 South Bridge



Item	Description
SB SATA Configuration	
OnChip SATA Channel	**Enable** (default) or **Disable** Serial ATA.
OnChip SATA Type	Select OnChip SATA Type ► Options: **Native IDE**, **AHCI** (default), **Legacy IDE** and **AHCI as ID 7804**
SB USB Configuration	
XHCI Controller	**Enable** or **Disable** (default) XHCI.
EHCI HC	**Enable** (default) or **Disable** EHCI Controller
USB Internal Port	**Enable** (default) or **Disable** USB Internal Port
HUB Port	**Enable** (default) or **Disable** USB Port

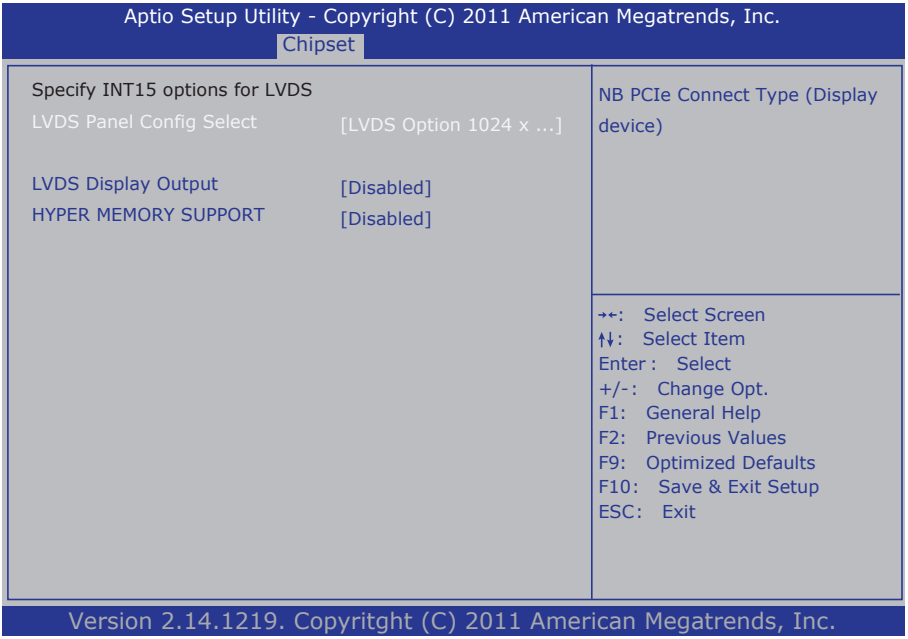
SB SD Configuration	
SD Mode	Configure SD mode: ► Options: **Disabled** (default), **ADMA, DMA** and **PIO.**
SD Trace Length	Configure Trace Length (inches): ► Options: **Less 6** (default), **Between 6 And 11** and **Greater 11**
SD Host Controller Version	Select Secure Digital (SD) Host Controller Version: ► Options: **SD 2.0** (default) and **SD 3.0**
SB HD Azalia Configuration	
HD Audio Azalia Device	Configure Azalia HD Audio Controller: ► Options: **Auto**, **Disabled** and **Enabled** (default)

3.3.2 North Bridge



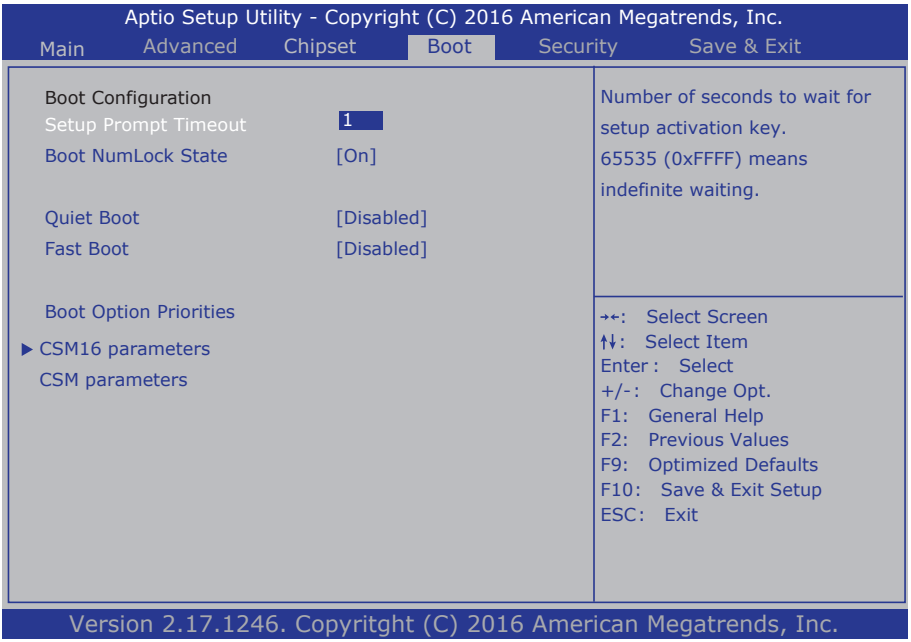
Item	Description
Socket 0 Information	View Information related to Socket 0

3.3.3 North Bridge LVDS Config Select



Item	Description
LVDS Panel Config Select	Select LVDS resolution. Default: **LVDS Option 1024 X 768 18Bit Single**
LVDS Display Output	**Enable** or **Disable** (default) LVDS Display Output
HYPER MEMORY SUPPORT	**Enable** or **Disable** (default) HYPER MEMORY SUPPORT

3.4 Boot

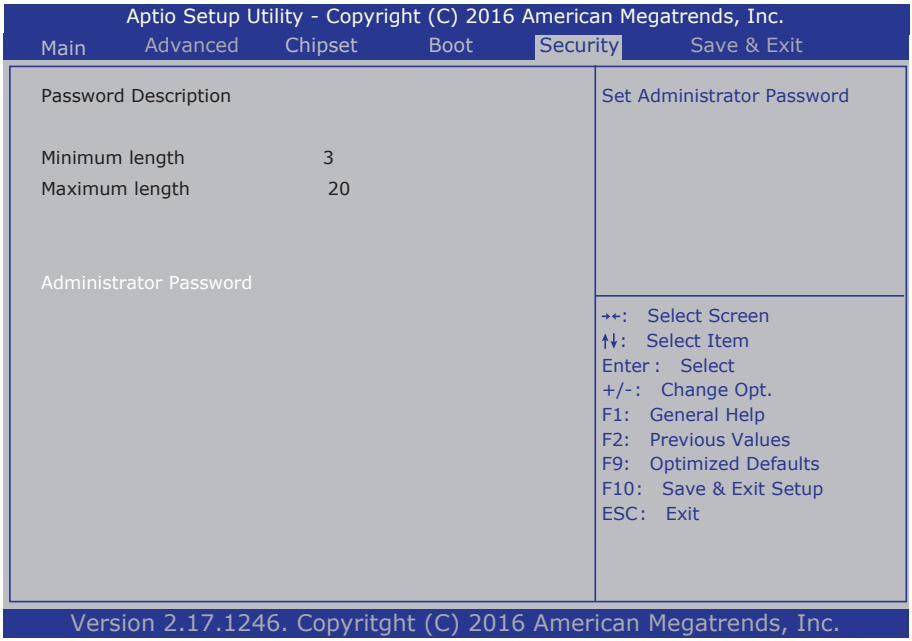


Item	Description
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Boot NumLock State	Select the keyboard NumLock state ► Options: **On** (default) and **Off**.
Quiet Boot	**Enable** or **Disable** (default) Quiet Boot option.
Fast Boot	**Enable** or **Disable** (default) boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.
CSM16 Parameters	
GateA20 Active	Configure GateA20 Active mode. Options: ► **Upon Request** (default): GA20 can be disabled using BIOS services. ► **Always**: Do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages	Set display mode for Option ROM. ► Options: **Force BIOS** (default) and **Keep Current**.
CSM parameters	
Launch CSM	Controls if CSM will be lanuched. ► Options: **Enabled** (default) and **Disabled**.
Boot option filter	Controls what devices system can boot to. ► Options: **UEFI and Legacy** (default), **Legacy only** and **UEFI only**.
Launch PXE OpROM policy	Controls the execution of UEFI and Legacy PXE OpROM. ► Options: **Do not launch** (default), **UEFI only** and **Legacy only**.
Launch Storage OpROM policy	Controls the execution of UEFI and Legacy Storage OpROM. ► Options: **Do not launch** (default), **UEFI only** and **Legacy only** (default).
Launch Video OpROM policy	Controls the execution of UEFI and Legacy Video OpROM. ► Options: **Do not launch** (default), **UEFI only** and **Legacy only** (default).
Other PCI device ROM priority	For PCI devices other than Network, Mass storage or Video defines which OpROM to launch. ► Options: **UEFI OpROM** (default) and **Legacy OpROM**.

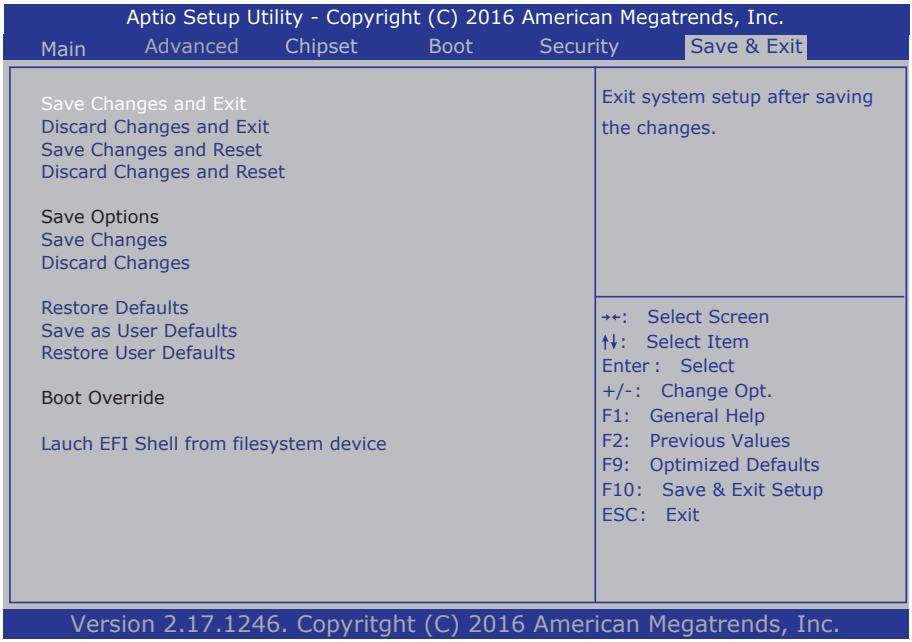
3.5 Security

The **Security** menu sets up the administrator password. Once an administrator password is set up, this BIOS SETUP utility is limited to access and will ask for the password each time any access is attempted.



Item	Description
Administrator Password	To set up an administrator password: 1. Select **Administrator Password**. The screen then pops up an **Create New Password** dialog. 2. Enter your desired password that is no less than 3 characters and no more than 20 characters. 3. Hit [Enter] key to submit.

3.6 Save & Exit



Setting	Description
Save Changes and Exit	Exit system setup after saving the changes. ► Enter the item and then a dialog box pops up: **Save configuration and exit? (Yes/ No)**
Discard Changes and Exit	Exit system setup without saving the changes. ► Enter the item and then a dialog box pops up: **Quit without saving? (Yes/ No)**
Save Changes and Reset	Reset the system after saving the changes.
Discard Changes and Reset	Discard the changes and reset the system
Save Changes	Save Changes done so far to any of the setup options.
Discard Changes	Discard Changes done so far to any of the setup options.

Restore Defaults	Restore/Load Default values for all the setup options. ► Enter the item and then a dialog box pops up: **Load Optimized Defaults? (Yes/ No)**
Save as User Defaults	Save the changes done so far as User Defaults.
Restore User Defaults	Restore the User Defaults to all the setup options.
Launch EFI Shell from filesystem device	Attempts to launch EFI shell application (Shell.efi) from one of the available filesystem devices.

3.7 AMI BIOS Checkpoints

3.7.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

3.7.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed

0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.

0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available

0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)

0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable

0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found

0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

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Appendix

Appendix A: I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
0x00000000-0x000003AF	PCI bus
0x00000000-0x000003AF	Motherboard resources
0x00000000-0x000003AF	Direct memory access controller
0x000003B0-0x000003DF	PCI bus
0x000003B0-0x000003DF	VgaSave
0x000003E0-0x00000CF7	PCI bus
0x00000D00-0x0000FFFF	PCI bus
0x0000F000-0x0000F0FF	Video Controller (VGA Compatible)
0x0000E000-0x0000EFFF	PCI standard PCI-to-PCI bridge
0x0000E000-0x0000EFFF	Standard Dual Channel PCI IDE Controller
0x0000E040-0x0000E047	Standard Dual Channel PCI IDE Controller
0x0000E030-0x0000E033	Standard Dual Channel PCI IDE Controller
0x0000E020-0x0000E027	Standard Dual Channel PCI IDE Controller
0x0000E010-0x0000E013	Standard Dual Channel PCI IDE Controller
0x0000D000-0x0000DFFF	PCI standard PCI-to-PCI bridge
0x0000D000-0x0000DFFF	Standard Dual Channel PCI IDE Controller
0x0000D040-0x0000D047	Standard Dual Channel PCI IDE Controller
0x0000D030-0x0000D033	Standard Dual Channel PCI IDE Controller
0x0000D020-0x0000D027	Standard Dual Channel PCI IDE Controller
0x0000D010-0x0000D013	Standard Dual Channel PCI IDE Controller
0x0000C000-0x0000CFFF	PCI standard PCI-to-PCI bridge
0x0000C000-0x0000CFFF	Ethernet Controller
0x0000F190-0x0000F197	Standard Dual Channel PCI IDE Controller
0x0000F180-0x0000F183	Standard Dual Channel PCI IDE Controller
0x0000F170-0x0000F177	Standard Dual Channel PCI IDE Controller
0x0000F160-0x0000F163	Standard Dual Channel PCI IDE Controller
0x0000F150-0x0000F15F	Standard Dual Channel PCI IDE Controller

0x0000F100-0x0000F10F	Standard Dual Channel PCI IDE Controller
0x000001F0-0x000001F7	Primary IDE Channel
0x000003F6-0x000003F6	Primary IDE Channel
0x00000170-0x00000177	Secondary IDE Channel
0x00000376-0x00000376	Secondary IDE Channel
0x00000A79-0x00000A79	ISAPNP Read Data Port
0x00000279-0x00000279	ISAPNP Read Data Port
0x00000274-0x00000277	ISAPNP Read Data Port
0x0000040B-0x0000040B	Motherboard resources
0x000004D6-0x000004D6	Motherboard resources
0x00000C00-0x00000C01	Motherboard resources
0x00000C14-0x00000C14	Motherboard resources
0x00000C50-0x00000C51	Motherboard resources
0x00000C52-0x00000C52	Motherboard resources
0x00000C6C-0x00000C6C	Motherboard resources
0x00000C6F-0x00000C6F	Motherboard resources
0x00000CD0-0x00000CD1	Motherboard resources
0x00000CD2-0x00000CD3	Motherboard resources
0x00000CD4-0x00000CD5	Motherboard resources
0x00000CD6-0x00000CD7	Motherboard resources
0x00000CD8-0x00000CDF	Motherboard resources
0x00000800-0x0000089F	Motherboard resources
0x00000B20-0x00000B3F	Motherboard resources
0x00000900-0x0000090F	Motherboard resources
0x00000910-0x0000091F	Motherboard resources
0x0000FE00-0x0000FEFE	Motherboard resources
0x00000370-0x00000371	Motherboard resources
0x000003E8-0x000003EF	Communications Port (COM3)
0x000002E8-0x000002EF	Communications Port (COM4)
0x00000290-0x0000029F	Motherboard resources
0x00000060-0x00000060	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard

0x00000064-0x00000064	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00000378-0x0000037F	Printer Port (LPT1)
0x00000020-0x00000021	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x00000081-0x00000083	Direct memory access controller
0x00000087-0x00000087	Direct memory access controller
0x00000089-0x0000008B	Direct memory access controller
0x0000008F-0x0000008F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller
0x00000040-0x00000043	System timer
0x00000070-0x00000071	System CMOS/real time clock
0x00000061-0x00000061	System speaker
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000044-0x0000005F	Motherboard resources
0x00000062-0x00000063	Motherboard resources
0x00000065-0x0000006F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x000004D0-0x000004D1	Motherboard resources
0x000000F0-0x000000FF	Numeric data processor
0x000003C0-0x000003DF	VgaSave

Appendix B: BIOS Memory Map

Address	Device Description
0xA0000-0xBFFFF	PCI bus
0xA0000-0xBFFFF	VgaSave
0xC0000-0xDFFFF	PCI bus
0x80000000-0xFFFFFFFF	PCI bus
0x68000000-0x7FFFFFFF	Motherboard resources
0xC0000000-0xCFFFFFFF	Video Controller (VGA Compatible)
0xFEB00000-0xFEB3FFFF	Video Controller (VGA Compatible)
0xFEB44000-0xFEB47FFF	Microsoft UAA Bus Driver for High Definition Audio
0xFEA00000-0xFEAFFFFF	PCI standard PCI-to-PCI bridge
0xFE900000-0xFE9FFFFF	PCI standard PCI-to-PCI bridge
0xFE800000-0xFE8FFFFF	PCI standard PCI-to-PCI bridge
0xFE800000-0xFE8FFFFF	Ethernet Controller
0xD0000000-0xD00FFFFF	PCI standard PCI-to-PCI bridge
0xD0000000-0xD00FFFFF	Ethernet Controller
0xFEB4F000-0xFEB4F3FF	Standard Dual Channel PCI IDE Controller
0xFEB4E000-0xFEB4EFFF	Standard OpenHCD USB Host Controller
0xFEB4D000-0xFEB4D0FF	Standard Enhanced PCI to USB Host Controller
0xFEB4C000-0xFEB4CFFF	Standard OpenHCD USB Host Controller
0xFEB4B000-0xFEB4B0FF	Standard Enhanced PCI to USB Host Controller
0xFEB40000-0xFEB43FFF	Microsoft UAA Bus Driver for High Definition Audio
0xFEC00000-0xFEC00FFF	Motherboard resources
0xFEE00000-0xFEE00FFF	Motherboard resources
0xFED80000-0xFED8FFFF	Motherboard resources
0xFED61000-0xFED70FFF	Motherboard resources
0xFEC10000-0xFEC10FFF	Motherboard resources
0xFED00000-0xFED00FFF	Motherboard resources

0xFED00000-0xFED00FFF	High precision event timer
0xFFC00000-0xFFFFFFFF	Motherboard resources
0xFEB4A000-0xFEB4AFFF	Standard OpenHCD USB Host Controller
0xFEB49000-0xFEB49FFF	Standard OpenHCD USB Host Controller
0xFEB48000-0xFEB480FF	Standard Enhanced PCI to USB Host Controller
0xE0000000-0xEFFFFFFF	System board
FED45000-FED8FFFF	Motherboard resources
FED90000-FED93FFF	Motherboard resources
FEE00000-FEEFFFFF	Motherboard resources
FF000000-FFFFFFFF	Intel(R) 82802 Firmware Hub Device
FF000000-FFFFFFFF	Motherboard resources

Appendix C: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 9	Microsoft ACPI-Compliant System
IRQ 11	Video Controller (VGA Compatible)
IRQ 19	Microsoft UAA Bus Driver for High Definition Audio
IRQ 19	PCI standard PCI-to-PCI bridge
IRQ 19	Standard Dual Channel PCI IDE Controller
IRQ 16	PCI standard PCI-to-PCI bridge
IRQ 16	Microsoft UAA Bus Driver for High Definition Audio
IRQ 17	PCI standard PCI-to-PCI bridge
IRQ 17	Standard Dual Channel PCI IDE Controller
IRQ 17	Standard Enhanced PCI to USB Host Controller
IRQ 17	Standard Enhanced PCI to USB Host Controller
IRQ 17	Standard Enhanced PCI to USB Host Controller
IRQ 18	PCI standard PCI-to-PCI bridge
IRQ 18	Standard Dual Channel PCI IDE Controller
IRQ 18	Standard OpenHCD USB Host Controller

IRQ 18	Standard OpenHCD USB Host Controller
IRQ 18	Standard OpenHCD USB Host Controller
IRQ 18	Standard OpenHCD USB Host Controller
IRQ 10	Ethernet Controller
IRQ 7	Communications Port (COM3)
IRQ 7	Communications Port (COM4)
IRQ 1	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
IRQ 12	Microsoft PS/2 Mouse
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 0	System timer
IRQ 8	System CMOS/real time clock
IRQ 13	Numeric data processor

Appendix D: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. Then, WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming. Below are the source codes written in C, please take them for WDT application examples.

C language Code

```
/*-----      Include Header Area -----*/
#include “math.h”
#include “stdio.h”
#include “dos.h”

/*-----      routing, sub-routing -----*/

void main()
{
/*-------- index port 0x2e ---------*/
            outportb(0x2e, 0x87);          /* initial IO port */
            outportb(0x2e, 0x87);           /* twice,  */

            outportb(0x2e, 0x07);           /* point to logical device */
            outportb(0x2e+1, 0x07);           /* select logical device 7 */
            outportb(0x2e, 0xf5);          /* select offset f5h */
            outportb(0x2e+1, 0x40);           /* set bit5 = 1 to clear bit5 */
            outportb(0x2e, 0xf0);          /* select offset f0h */
            outportb(0x2e+1, 0x81);           /* set bit7 =1 to enable WDTRST# */
            outportb(0x2e, 0xf6);          /* select offset f6h */
            outportb(0x2e+1, 0x05);           /* update offset f6h to 0ah :10sec */
            outportb(0x2e, 0xf5);          /* select offset f5h */
            outportb(0x2e+1, 0x20);           /* set bit5 = 1 enable watch dog time */

            outportb(0x2e, 0xAA);           /* stop program F71869E, Exit */
}
```

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