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IC-FEP-VPX3d

Kintex® UltraScale™ FPGA 3U VPX board with FMC+ Site

- *1*Kintex® UltraScale™ FPGA*
- *2* DDR4 banks (up to 4GB each)*
- *1*Artix-7 control node*
- *1*FMC+ site (VITA 57.4)*

Based on the latest Xilinx 20nm FPGA family, the **IC-FEP-VPX3d** enhances the front-end processing (FEP) product line of Interface Concept.

By offering a better performance/power consumption ratio compared to the previous FPGA, the Kintex® UltraScale™ FPGA makes the **IC-FEP-VPX3d** the perfect solution to applications requiring DSP intensive processing in a 3U VPX form factor.

The **IC-FEP-VPX3d** and the other building blocks (Intel® and PowerPC SBCs, Ethernet Switches & Routers, FMC) running our Signal Processing Reference Design are the ideal platforms for customers who want to streamline development by concentrating their efforts on their most strategical tasks.

Description

The **IC-FEP-VPX3d** takes advantage of Kintex® UltraScale™ family capabilities and features by offering the users: scalability, performance, connectivity and reliability versus the environment.

The Kintex® UltraScale™ built on a high performance, low power 20nm process technology are available in multiple models providing different features while keeping the same packages and footprint. Hence, the **IC-FEP-VPX3d** is available with a selection of 3 FPGA (KU060, KU085 or KU115), and speed grades 1, 2 & 3.

The FPGA 2133MB/s bus interfaces with the 2 DDR4 banks remove bottleneck in DSP and packet processing, maximizing the board transfer performance. The Fabric Links of the VPX backplane are connected to the FPGA GTHs (FPGA dependent) transceivers, allowing data rate up to 16.3 Gbps, and up to 32 differential pairs.

The Embedded Hard IP Resources can be used to implement PCI Express Gen2/Gen3 (FPGA dependent) links, as well as the 10 Gigabit Ethernet ports (XAUI, 10GBase-KR).

The FMC+ site of the **IC-FEP-VPX3d** is compliant with the FPGA Mezzanine Card standard (VITA 57.4), allowing the installation of FMC modules provided by IC or developed by the users.

The **IC-FEP-VPX3d** benefits from the latest enhancements of Kintex® UltraScale™ regarding the power reduction and is available from standard, air-cooled to conduction-cooled grades (85°C).

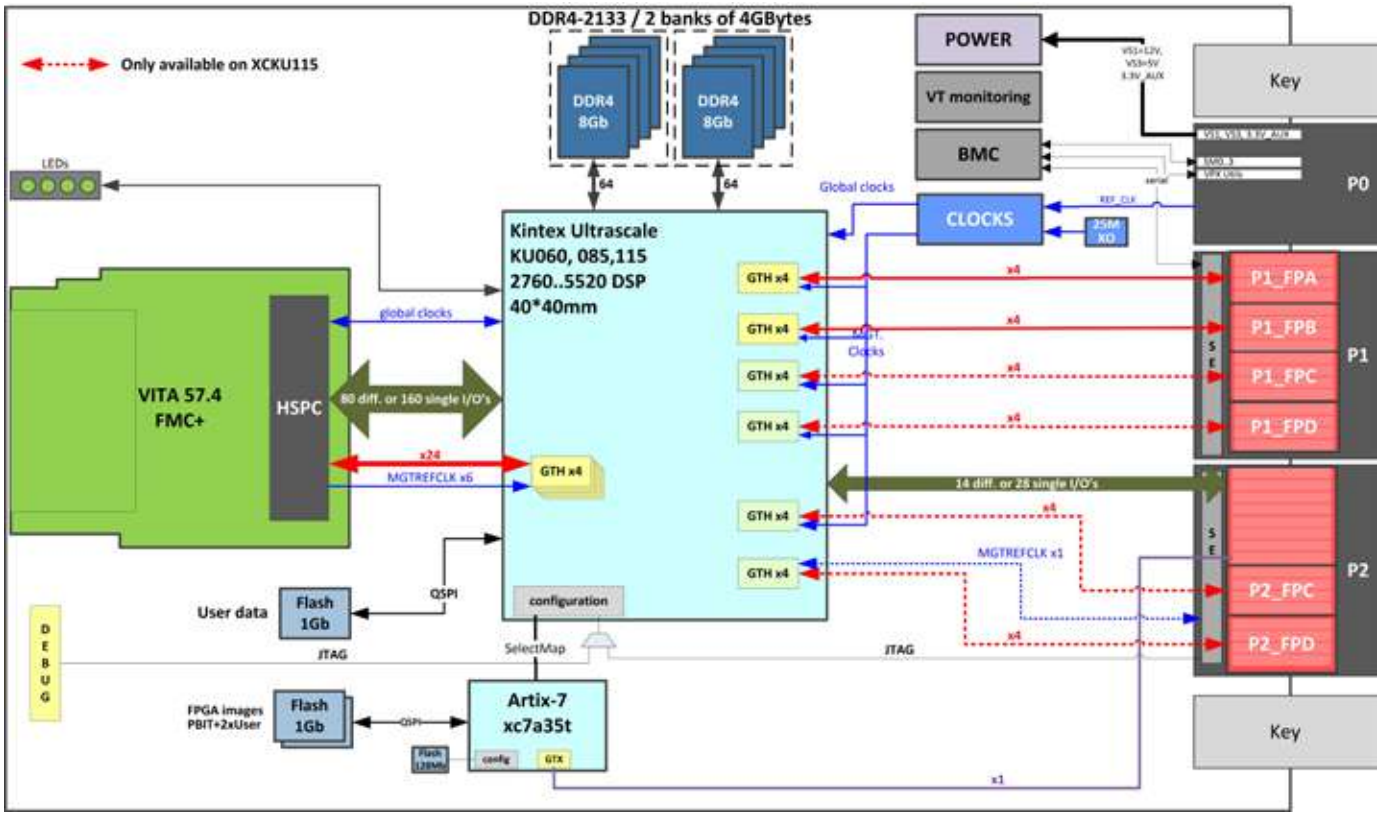
Furthermore, Kintex® UltraScale™ interfaces with a flash for local storage of up to 2 bitstreams. It supports secured bitstreams and partial reconfiguration.

Due to the modularity of the FPGA, the **IC-FEP-VPX3d** is compliant with several Module Profiles of the OpenVPX standard (TBD).

The **IC-FEP-VPX3d** is a 3U VPX board compliant with 3U module definitions of the VITA 46.0 standard.

It is available in air-cooled and conduction cooled versions compliant with VITA 47 classes

Block Diagram



Main features

Processing Unit
- Kintex® UltraScale™ KU060, KU85 or KU115
- Two banks of DDR4: 64-bit wide, up to 4GB each
- 3 * 128 MBytes of QSPI flash (bitstreams storage)
- 1 * 128 MBytes of QSPI flash (User Data storage)

VPX Interfaces
- Four 4-lanes fabric ports on P1/P2
  - 4 * GTH x4 (Fat Pipes P1A, P1B, P1C (*) & P1D (*))
  - 2 * GTH x4 (Fat Pipes P2C (*) & P2D (*))
  (*) depending on FPGA models
- General purpose IOs
- 14 differential pairs from FPGA onb P2

FMC+ VITA 57.4 interfaces
- 4 + 2 GTH x4 links
- 80 or 160 differential pairs
- 6 reference clocks

Miscellaneous
- PIC µ-controller for System Management to VITA 46.11
- 8 LEDs
- Configuration switches

Accessories
- Engineering kit : JTAG ports for direct FPGA configuration
- Rear Transition Module

Interface features

P0 connector
- VS3, 3V3_AUX, VS1 (+12V for FMC)
- REF_CLK
- I2C bus, utilities (SYSRESET, NVMRO, GAx)

P1 connector
- four 4-lanes fabric ports
- 16GTH(*) (ports A, B, C & D)
- RS232 (PIC µC)
- GPIOs - user defined

P2 connector
- two 4-lanes fabric ports
- 8GTH(*) (ports C & D)
- General purpose I/O (on P2)
- 14 differential pairs

FMC connector
- 24 GTH(*)
- 80 or 160 differential pairs
- 6 clocks (LVDS Diff)

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On-board firmware

The **IC-FEP-VPX3d** hardware platform is compatible with Xilinx development tools Vivado TM , Platform cable, etc.

Interface Concept provides

- VHDL code for system services (DDR4, PCIe, Aurora, IC FMC interfaces, etc.) and reference designs such as PCIe DMA Engine, signal capture & processing, etc.
- Host drivers for our CPU (Linux, VxWorks)

Customers can implement their own real-time applications with the capability to integrate existing Open Source code or third-party IP cores.

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Grades

Criterion	Coating	Operation Temperature	Rec. Airflow	Oper. HR% no cond.	Storage Temperature	Sinusoidal Vibration	Random Vibration	Shock 1/2 Sin. 11ms
Standard	Optional	0 to 55°C	1 .. 2 m/s	5 to 90%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Extended	Yes	-20 to 65°C	2 .. 3 m/s	5 to 95%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Rugged	Yes	-40 to 75°C or 85° C(*)	2 .. 5 m/s	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction Cooled	Yes	-40 to 75°C or 85° C at the thermal interface(*)		5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.1g2 /Hz [10..2000]Hz	40G

(*) : For some architectures, subject to limitation (or extension) depending on Frequency restriction / Processing usage rate. Consult us for more information.

All information contained herein is subject to change without notice.

For more information, please contact:

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