PROPRIETARY NOTICE

emPC-CXR

rugged embedded PC

(Hardware Manual)

Version V1.4

refers to product revision no.
V1.0

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About this Manual

This is the hardware manual for the emPC-CXR rugged embedded PC.

Conventions

If numbers are specified in this manual, they will be either decimal or hexadecimal. We use C-notation to identify hexadecimal numbers (the 0x prefix).

If we refer to low active signal names, they will suffixed by a "#" character.

Some parts of the contains notices you have to observe to ensure your personal safety, or to prevent damage to property. These are visually marked with the following alert symbols:

DANGER

Indicates that death or severe personal injury *will* result if proper precautions are not taken.

WARNING

Indicates that death or severe personal injury *may* result if proper precautions are not taken.

CAUTION

Indicates that *minor* personal injury can result if proper precautions are not taken.

NOTICE

Indicates that damage to equipment can result if proper precautions are not taken.

Indicates information that we think you should have read to save your time by avoiding common problems. Important suggestions that should be followed will also be marked with this sign.

Acronyms and Abbreviations

EMC	Electromagnetic capability.
ESD	Electrostatic discharge.
GND	System ground potential. Inside the product this is connected to the metal housing, which might be connected to protective earth by the installation. There exist some isolated reference grounds for communication interfaces or IO. These reference signals are referred to as GND-x, where x indicates function.

1 Introduction

1.1 Features

1.1.1 Hardware

- COM Express Processing Core
  - Intel Core i7-3517UE
  - Intel Celeron 1047UE
- DDR3 memory as defined by COM Express Module
- Internal mSATA socket for SATA based SSD modules
- 2 x 10/100/1000 Mbit/s Ethernet on M12 connector
- 2 x USB interface on M8 connector
- 128 kB of nvSRAM (which does not require battery backup)
- Battery backed up RTC
- COM express internal watchdog function
- Power supply/temperature monitoring
- VGA display connector D-SUB
- Two 5 pin M12 connectors for serial ports. Customizable as:
  - CAN (isolated)
  - RS232/RS485 (isolated)
- 4 digital IO (in/out) on M12 connector (isolated, externally powered)
- System Power supply 9..34 VDC on M12 connector
- Power LED
- Optional 2x16 character display and user defined buttons

1.1.2 Software

Supported by

- Windows 7
- Windows 7 embedded
- Linux

Contact Janz Tec for more information about the available software packages.

1.2 Functional Overview

The functional components of the product are shown in figure 1.

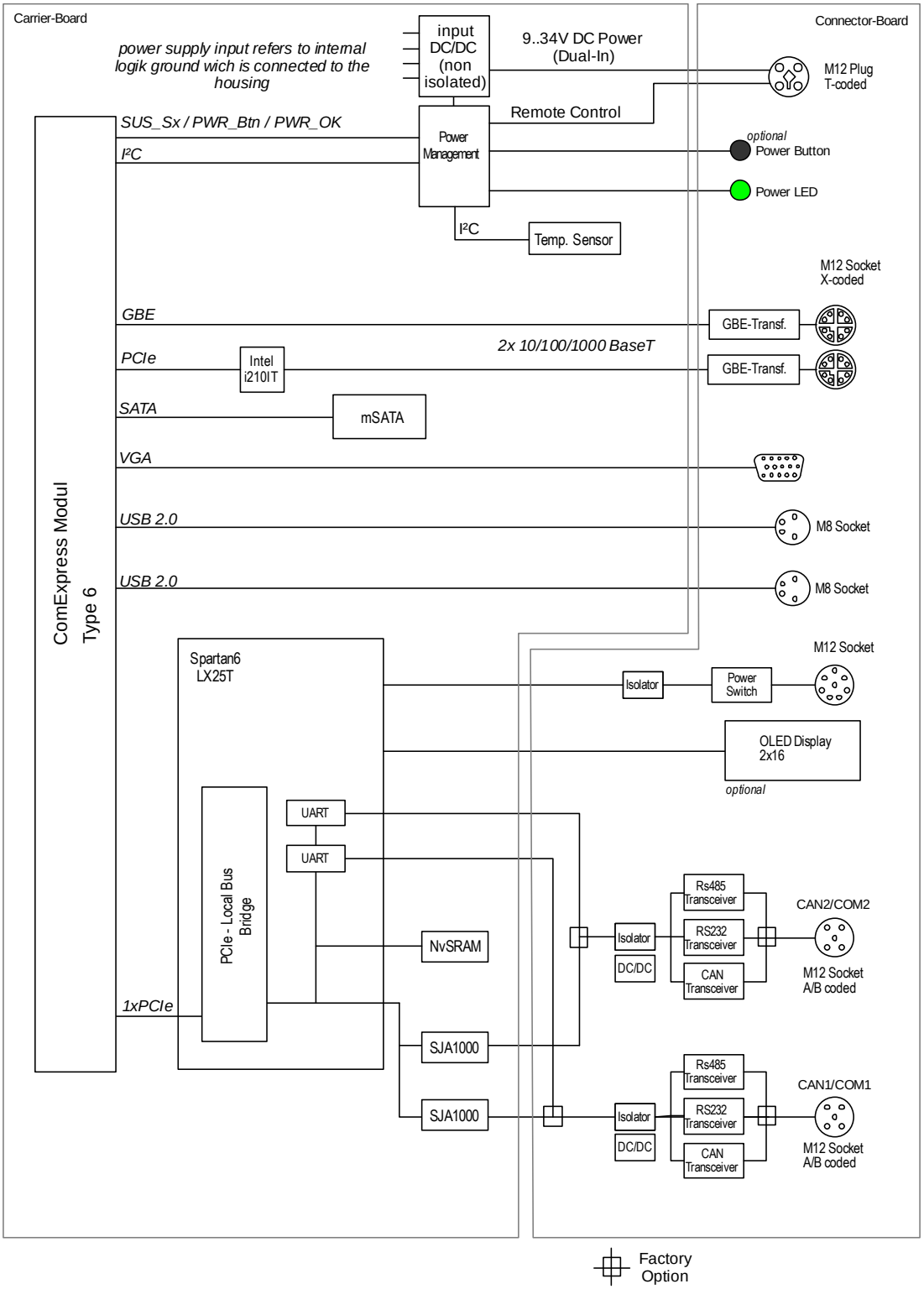


figure 1: block diagram

2 Safety Instructions

Refer to page iv for explanation of the warning notice system.

The product described in this documentation may be operated only by personnel qualified for the specific task in accordance with the relevant documentation for the specific task, in particular its warning notices and safety instructions. Qualified personnel are those who, based on their training and experience, are capable of identifying risks and avoiding potential hazards when working with these products.

2.1 Installation and Maintenance

The power supply of the product operates with hazardous voltages.

DANGER: Electrical Shock

Danger to life.
This product operates with 9..34 V DC SELV power supply. Do *not* connect this product to an improper power supply (No AC power, no more than 34 V DC or no non-SELV circuit)!

DANGER: Electrical Shock

Danger to life.
The IO interfaces (connectors) of the product are only suited to be connected to SELV circuits. Use interfaces (connectors) for their intended use only.
This product must not be connected to telecommunication networks (TNV circuits).

CAUTION: Explosive Risk

The installed computer board is equipped with a Lithium battery.
Danger of explosion if battery is incorrectly replaced. Replace only with battery of the same or equivalent type.

CAUTION: Fire Risk

The digital IO must be powered by a SELV power supply, that complies with the requirements of a limited energy source (LPS) (By using an appropriate supply or an external fuse).

WARNING: Burns Hazard

The product generates considerable amount of heat. The housing transports this heat to the environment and therefore gets hot. **Caution when touching the housing, burns hazard**!

To comply with UL/IEC/EN 60950-1: If the product is not supplied by a limited current circuit, then a disconnection means - easily accessible and identifiable - has to be provided in the final installation to separate the equipment from all power sources.

2.2 Ambient and Environmental Conditions

CAUTION: Damage

Do not operate the product beyond the specified ambient conditions

DANGER: Explosive Risk

Do not operate the product in potentially explosive atmosphere..

NOTICE: EMI

This product is a class A device. This product may cause radio interference. In this case the user must take adequate measures.

NOTICE

UL Applications: For outdoor use, the product has to be mounted in a suitable electrical enclosure complying with enclosure requirement of UL50, UL50E and the max. supply voltage shall be 30VDC in normal and single fault condition to comply with voltage requirements of UL60950-2-22.

3 Installation

CAUTION

The product is designed as a fan less computer system. Nevertheless a certain amount of heat is generated inside the housing. The housing transports this heat to the environment. **Caution when touching the housing, burns hazard**!

The product can be operated with DC power supply from 9 to 34 V.

3.1 Mounting

The emPC-CXR is intended to be mounted on a flat surface wall.

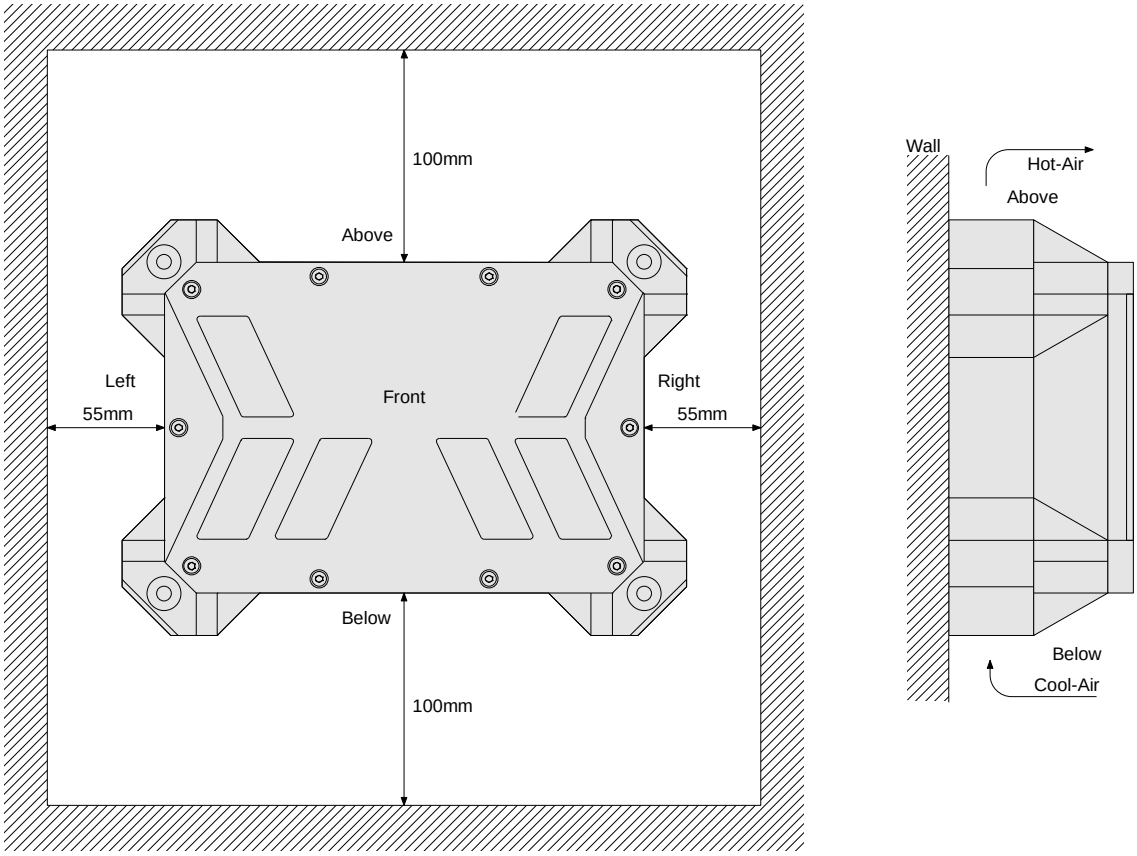


figure 2: Mounting guidelines

NOTICE

The product must be mounted exactly as indicated in figure 2 to allow the required natural heat transfer. Derivations of < 5 ° do not matter.
The indicated area must be free of obstacles which prevent heat transfer.
There should be no space between the wall and the product (use no spacers for mounting).

NOTICE

The ambient temperatures **below**, **left**, **right** and in **front** of the product must not exceed the specified maximum ambient temperature.

3.1.1 Mounting Screws

The product must be mounted with M6 Screws with appropriate washers. Stainless steel is recommended in harsh environment. The washers may have a maximum diameter of 15 mm.

3.1.2 Mounting Wall

NOTICE

The mounting wall must have enough structural integrity at high temperatures. The Case temperature of the product will be approximately 15 K higher than the ambient temperature.

3.2 Connectors and Operators

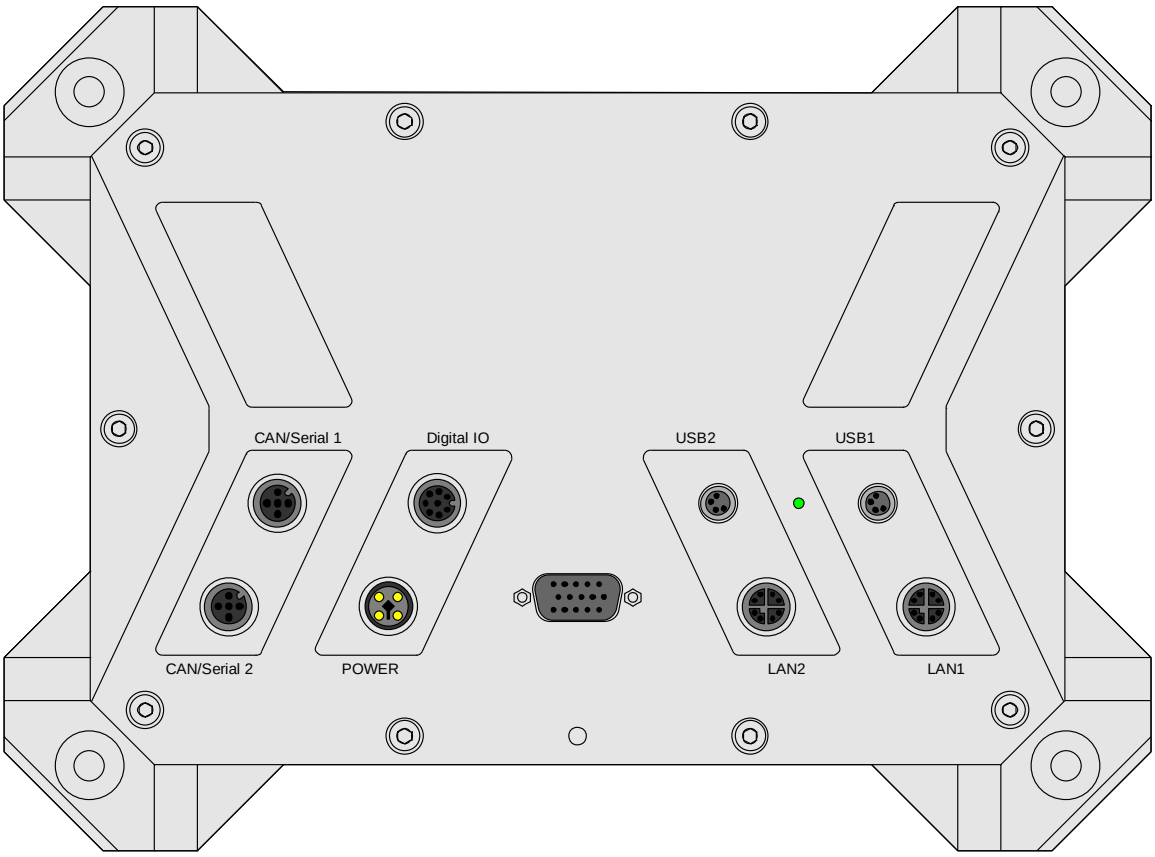


figure 3: front view with connectors

Below the VGA connector you find an M5 thread for an additional earth connection. EMI Tests were passed without extra earth connection. However, during EMI testing, earth connection was established with the shields of the IO cables (VGA, LAN, …).

The green power LED between the USB connectors lights when the system is running. It does not light when the system is in power down mode even if power is applied at the power connector.

NOTICE
Do not actuate connectors when power is applied.

NOTICE
All connectors (M12/M8/DSUB) are not sealed when no mating connector is present. Use a screw plug to seal unused connectors.

NOTICE
Mechanical actuation of M12/M8 connectors is prohibited below -25 °C.

3.2.1 POWER IN

The system power supply is connected with a 4 pin T-coded M12 male connector.

4 pin male M12 T-coded

1	VIN-A (9..34V DC)
2	VIN-B (9..34V DC)
3	VS
4	GND

table 1: Power supply connector

DANGER

The product may only be operated with power supplies which can be considered SELV circuits.

The return of the power supply (pin 4 = GND) is connected to the internal system GND (via EMI filter chokes). The internal system GND is connected to the housing internally. Hence the shells of all connectors are on system GND potential.

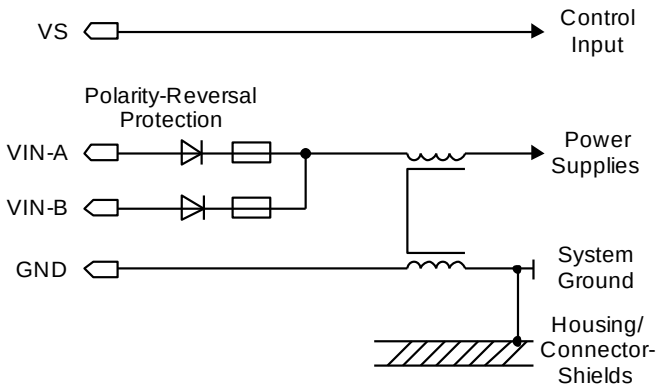


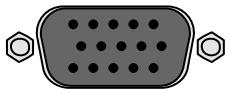
figure 4: Power Supply Input

To comply with UL/IEC/EN 60950-1 : If the product is not supplied by a limited current circuit, then a disconnection means - easily accessible and identifiable - has to be provided in the final installation to separate the equipment from all power sources.

The specified power supply voltage range is defined at the input connector of the product. At low input voltage and high system load, a high input current of several ampere will flow. This can lead to substantial drop on the power input cable (even when using 1.5 mm² M12 cable assemblies).

3.2.2 VGA connector

Analog VGA graphics connector as supplied by the COMexpress module.



15 pin female HD-Sub

1	Red	9	+5V
2	Green	10	GND
3	Blue	11	N/C
4	N/C	12	DDC Data
5	GND	13	HSync
6	GND	14	VSync
7	GND	15	DDC Clock
8	GND		

table 2: VGA connector

3.2.3 Ethernet Interfaces LAN1 and LAN2

Ethernet interfaces of the motherboard. The Ethernet physics is 10/100/1000BaseT, available through the shielded M12 connectors.

8 pin female M12 X-coded

1	MDI0+	5	MDI3+
2	MDI0-	6	MDI3-
3	MDI1+	7	MDI2+
4	MDI1-	8	MDI2-

table 3: Ethernet connector

3.2.4 USB 2.0 Host Interfaces USB1 and USB2

2 USB 2.0 host interfaces are available through 4 pin M8 female connectors.

4 pin M8

1	+5V (red)
2	USB- (white)
3	GND (black)
4	USB+ (green)

table 4: USB connector with USB cables colour codes

The USB connectors do not provide standby power, thus wake on USB is not possible.

3.2.5 CAN

If the product is equipped with CAN interface(s), 5 pin A-coded M12 female connectors are equipped for the CAN.

5 pin female M12 A-coded

1	NC
2	NC
3	GND-CAN
4	CAN-H
5	CAN-L

table 5: M12 CAN connector

3.2.6 RS485

If the product is equipped with RS485 interface(s), 5 pin B-coded M12 female connectors are equipped.

5 pin female M12 B-coded

1	NC
2	DM (A)
3	GND-RS485
4	DP (B)
5	NC

table 6: M12 RS485 connector

3.2.7 RS232

If the product is equipped with RS232 interface(s), 5 pin B-coded M12 female connectors are equipped.

5 pin female M12 B-coded

1	RTS (out)
2	TxD (out)
3	GND-RS232
4	RxD (in)
5	CTS (in)

table 7: M12 RS232 connector

3.2.8 Digital IO

4 digital IO signals are available on 8 pin A-M12 female connector.

8 pin female M12 A-coded

1	VIN-DIO (10..34V DC)
2	DIO4
3	DIO3
4	DIO2
5	DIO1
6	NC
7	NC
8	GND-DIO

table 8: M12 RS232 connector

CAUTION

The digital IO must be powered by a SELV power supply, that complies with the requirements of a limited energy source (LPS) (By using an appropriate supply or an external fuse).

Digital IO pins drive VIN-DIO to the output pins (high side switch). Each digital IO pins can be read back so that it can be used as input as well. See figure 5 for details.

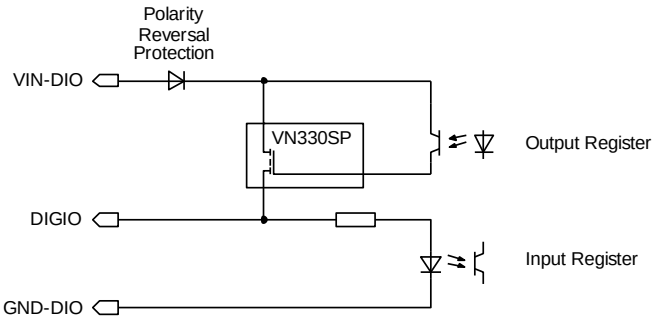


figure 5: DIO structure

Each port pin (DIO1…DIO4) is able to source 500mA into a load. The sum of all output currents should be limited to 1A.

NOTICE

When outputs are turned on, they source power from VIN-DIO to the output pin. If you use a pin as input, make sure you never turn on the corresponding output. Damage to the driving source may happen otherwise.

3.3 Application Hints

3.3.1 Right Angle Cable

When using right angle M8/M12 connectors, you have to obey the exit direction of the cables when planning the cabling. In figure 6 you find an example with all right angle cables.

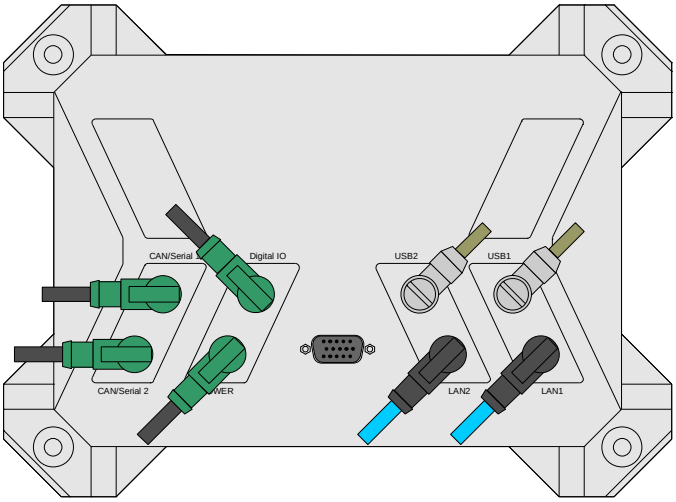


figure 6: right angle cable example

3.3.2 M12 Y Adapters

For applications with fieldbus connections that need to pass-through, Y-adapters can be used to provide two sockets for in-coming and out-going cables.

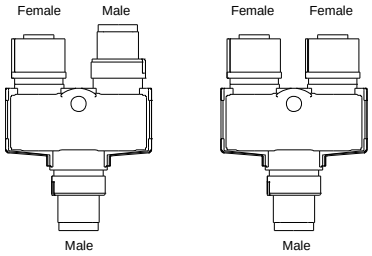


figure 7: M12 Y-connectors

Examples or such adapters are found below:

- M12 5pol A-coded male to female/male: Phoenix Contact SAC-5PY-M/F-M VP SH.
- M12 5pol A-coded male to female/female: Phoenix Contact SAC-5PY-M/2XF VP SH.

4 Maintenance

NOTICE

Always follow common ESD practice when you service the product!

All serviceable parts can be reached by removing the top cover of the product.

Task	Top Cover		Remarks
Replace mSATA	remove		
Replace Battery	remove		

NOTICE

All cables should be removed before removing the top cover.

4.1 Handling Top Cover

To remove/install the top cover, you need a Torx-T20 tool. A stainless steel tool is preferred.

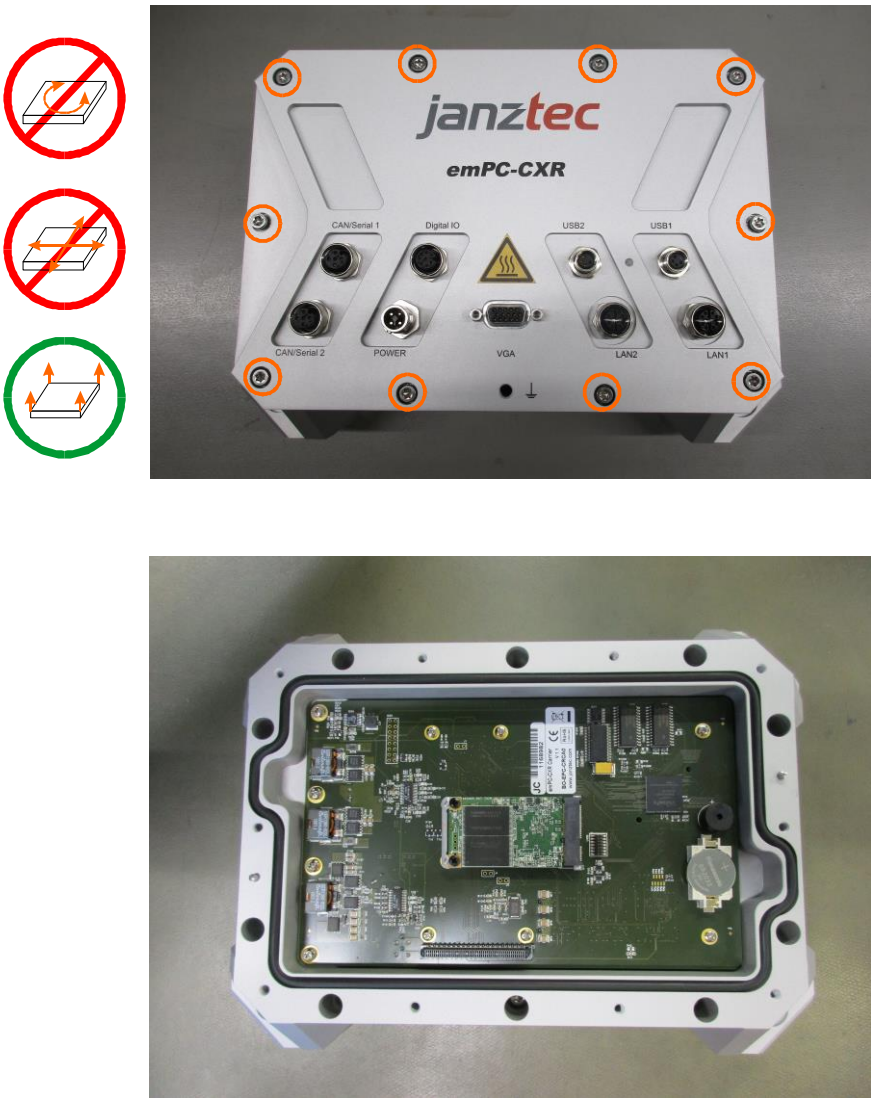


figure 8: Handling the Top Cover

To remove the top cover, refer to the following instructions:

- Remove the 10 top cover screws as indicated in figure 8
- Lift of the top cover in direction of the screws. Do not apply force in any other direction (rotation, horizontal force), else you might damage the internal high density connector which connects the connectors to the main board.
- Obey that you do not damage the connectors and components on the front panel PCB when you handle the removed top cover.

To install the top cover, refer to the following instructions:

- Check that the sealing is properly installed in its groove
- If IP67 is required, check the integrity of the sealing. If it is damaged, the sealing can be removed and replaced.
- Put the cover onto the housing, gently assigning the high density connector.
- Re-Apply all screws (including the contact washer). Recommended torque: 2.6 Nm.

4.2 Battery Replacement

CAUTION

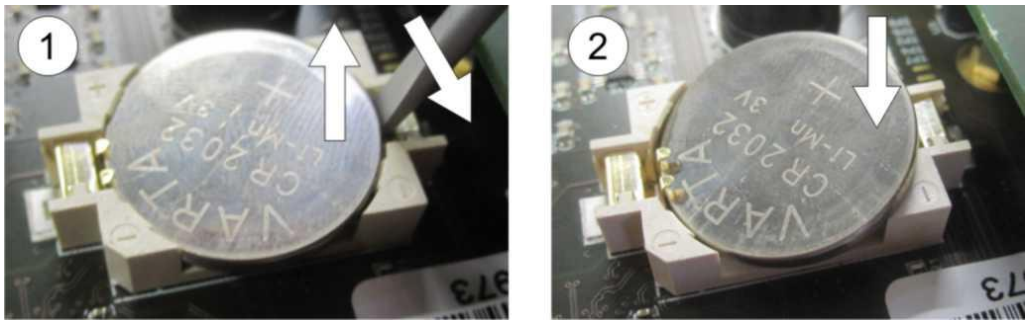
The installed computer board is equipped with a Lithium battery.
Danger of explosion if battery is incorrectly replaced. Replace only with battery of the same or equivalent type (3-volt lithium coin cell battery).

- Do not attempt to recharge the battery.
- Do not disassemble, crush, puncture, short external contacts, or dispose of in fire or water.

Compatible battery type: BR2032 (3 Volt lithium coin cell battery)

The battery is used for backing up the system time when the power supply is removed.

1. Turn off the computer properly through the operating system, then turn off any external devices.
2. Disconnect the power supply from the power connector.
3. Remove the top cover from the product and locate the battery on the system main board
4. Remove the battery from the holder (See figure 9)
5. Insert the new battery (See figure 9)
6. Reinstall the top cover



1. Removal: Insert screwdriver at right side and bend so that the battery pops outs. Use only gentle force, otherwise the battery holder might be damaged.
   The use a plastic tool is preferred to avoid shorting the battery
2. Insertion: Align new battery to the left side of the holder and gently press down on the right side of the battery until the battery snaps into the holder.

figure 9: Removing and replacing coin cell battery

4.3 mSATA

After inserting the mini card into the connector, it must be pushed down and locked with two M2,5 screws.

NOTICE

- The insertion depth of the screws that lock the PCI express mini card must not exceed 3.2mm.
- Make sure that the diameter of the screw or the washer does not make contact

	with components or traces on the mini card. Some cards have components very near to the mounting holes.

The mSATA socket only accepts SATA based SSD modules. It does not support PCI express based modules/cards.

5 Hardware details

5.1 PCI Express

The emPC-CXR uses PCI Express for a couple of expansion options. Some COM Express modules only provide a limited number of PCI Express lanes. Refer to Table 9 for a detailed resource list.

COM Express PCIe lanes	Function
PCIE0	Ethernet 2
PCIE1	FPGA
PCIE2	unused
PCIE3	unused
PCIE4	unused
PCIE5	unused
PCIE6	unused
PCIE7	unused

Table 9: COM Express PCIe lane usage

5.2 Ethernet

The emPC-CXR provides two 10/100/1000 ethernet interfaces

5.2.1 LAN1

This Ethernet interface is provides by the COM Express module, refer to the module documentation for details (e.g. controller type).

Wake on LAN implementation depends on the COM Express modules and is usually possible.

5.2.2 LAN2

This Ethernet interface is implanted on the carrier board by an Intel i210 ethernet controller.

The standard configuration uses the i210's iNVM memory for parameter storage. As an option, external FLASH memory option is possible, but not normally equipped on the carrier board.

Wake on LAN is not supported by Ethernet 2.

6 FPGA expansion subsystem

The PCIe interface for special Janz Tec Features is implemented by a FPGA and is identified by a set of IDs in PCIe configuration space as listed below:

Purpose	Value	Found in
Vendor ID	0x13C3	CFG space register 0x00
Device ID	0x2A00	CFG space register 0x02
Subsystem Vendor ID	0x13C3	CFG space register 0x2C
Subsystem ID emPC-CXR	0x2A00	CFG space register 0x2E

Table 10: PCI identification

The FPGA PCIe interface provides access to several register spaces.

PCI base address register	Description	Size
0	Local configuration registers (memory mapped)	512 B
1	N/A	-
2	CAN/RS232 address space	8 kB
3	Reserved	8 kB
4	Control registers	4 kB
5	NVRAM / IO port address space	1 MB

Table 11: Local address spaces

The actual addresses for these memory spaces are configured by the BIOS of your system every time the computer is booted. If you wish to access one of these spaces, then you need to read the actual addresses from the PCIe configuration space.

6.1 Control Registers

Address Offset	access	Description
BAR4 + 0x00	RO	INT_STAT
BAR4 + 0x04	RO	INT_MASK
BAR4 + 0x08	WO	INT_DISABLE
BAR4 + 0x0C	WO	INT_ENABLE
BAR4 + 0x10	WO	RESET_ASSERT
BAR4 + 0x14	WO	RESET_DEASSERT
BAR4 + 0x18	RO	RESET_STATUS
BAR4 + 0x1c	RW	I2C_CONTROL
BAR4 + 0x20	RO	FEATURE1
BAR4 + 0x24	RO	FEATURE2
BAR4 + 0x30	RW	TESTREG
BAR4 + 0x3C	RO	REVISON

Table 12: Control registers

6.1.1 Feature detection

FEATURE1 **BAR4 + 0x20 (32bit, ro)**

31..10	9	8	7..2	1	0
reserved	COM1	COM0	Reserved	CAN1	CAN0

CAN[1..0] High if corresponding CAN is available
COM[1..0] High if corresponding COM is available
Reserved Reserved positions are zero

REVISION **BAR4 + 0x3c (32bit, ro)**

31..24	23..16	15..8	7..0
ID	Reserved	Release	Build

ID Refers to the specific hardware design (0x02 is emPC-CXR)
Reserved Is 0x00
Release Specifies the current Version of the design
Build Running Build Number

6.1.2 Interrupt programming

The FPGA generate an interrupt that is logically or'ed amoung all internal interrupt sources.

To determine which source has generated an interrupt the Interrupt handler must read the interrupt status register:

INT_STAT **BAR4 + 0x0 (32bit, ro)**

31..10	9	8	7..2	1	0
reserved	COM1	COM0	Reserved	CAN1	CAN0

CAN[1..0] Interrupt status info. Each defined bit in this register reflects the status of the INT# pin of the corresponding CAN. A zero will be read when an interrupt is pending.

If a CAN interrupt request line is disabled, then the corresponding bit is forced to “1”.

COM[1..0] Interrupt status info. Each defined bit in this register reflects the status of the INT# pin of the corresponding COM. A one will be read when an interrupt is pending.
If a COM interrupt request line is disabled, then the corresponding bit is forced to “0”.

Reserved Reserved positions are undefined, and must not be considered. Software must mask them off.

Interrupt requests can be masked off by the CPU. This is done through the interrupt disable/enable registers. Interrupts are disabled after RESET, and you need to enable a CAN interrupt line before using it.

INT_ DISABLE **BAR4 + 0x8 (32bit, wo)**

31..10	9	8	7..2	1	0
reserved	COM1	COM0	Reserved	CAN1	CAN0

INT_ENABLE **BAR4 + 0xC (32bit, wo)**

31..10	9	8	7..2	1	0
reserved	COM1	COM0	Reserved	CAN1	CAN0

CAN[1..0] Writing one of the bits disables/enables interrupts from the corresponding
COM[1..0] function. Both registers are accessed in hot-1 technique: Writing a one to a bit disables/enables further interrupts from the corresponding function, writing zero to a bit do not affect the interrupt mask status of that function.
If a functions interrupt request line is disabled, then this functions interrupt bit will never appear in the INT_STAT register and it will not cause interrupts.

Reserved Reserved bit positions must be written as zero.

6.1.3 Function Reset

To ensure a defined state of a function at any time, it is possible to activate the RST# line of a function via software. This can be done with the reset assert/deassert registers. The RST# line of all functions are activated during a PCIe bus reset.

RESET_ASSERT **BAR4 + 0x10 (32bit, wo)**

31..10	9	8	7..2	1	0
reserved	COM1	COM0	Reserved	CAN1	CAN0

RESET_DEASSERT **BAR4 + 0x14 (32bit, wo)**

31..10	9	8	7..2	1	0
reserved	COM1	COM0	Reserved	CAN1	CAN0

CAN[1..0] Writing one of the bits disables/enables interrupts from the corresponding
COM[1..0] function. Both registers are accessed in hot-1 technique: Writing a one to a bit disables/enables further interrupts from the corresponding function, writing zero to a bit do not affect the interrupt mask status of that function.
If a functions interrupt request line is disabled, then this functions interrupt bit will never appear in the INT_STAT register and it will not cause interrupts.

Reserved Reserved bit positions must be written as zero.

6.1.4 Internal I²C bus

The control register for the onboard I²C interface provides bit-bang style I2C implementation.

I2C_CONTROL **BAR4 + 0x1c (32bit, rw)**

31..10	9	8	7..2	1	0
reserved				SCL	SDA

SDA I²C bidirectional data line.
Writing 0 sets the data line to low potential.
Writing 1 tristates the data line. An external pull-up resistor (1kOhm) raises the line to high potential. This must be done before reading data.

SCL I²C "bidirectional" clock line.
Writing 0 sets the clock line to low potential.
Writing 1 tristates the clock line. An external pull-up resistor (1kOhm) raises the line to high potential. This must be done before reading clock status.

Reserved Reserved bit positions must be written as zero.

6.2 CAN Interface

6.2.1 CAN address space

The CAN controllers are mapped into memory address space

Address Offset	accesses:
BAR2 + 0x000..0x0ff	CAN controller 0 registers (SJA1000)
BAR2 + 0x100..0x102	CAN controller 0 control
BAR2 + 0x200..0x2ff	CAN controller 1 registers (SJA1000)
BAR2 + 0x300..0x302	CAN controller 1 control

Refer to SJA1000 manual for description of registers and operation.

6.2.2 CAN termination and LEDs

Besides the registers of the SJA1000 (which are defined in the SJA1000 Manual), there are two additional registers which control the line termination and the front panel LEDs. These registers are unique for each channel.

CAN_TERM0,1 **BAR2 + 0x100, 0x300 (byte, rw)**

7	6	5	4	3	2	1	0
reserved							TERM
RESET:							
-							0

TERM Set to zero to disable the line-termination, Set to one to enable the termination resistor.

Reserved Reserved positions should not be changed. You should use read-modify-write operation to change this register.

CAN_LED0,1 **BAR2 + 0x102, 0x302 (byte, wo)**

7	6	5	4	3	2	1	0
reserved						LEDG	LEDR
RESET:							
-						0	0

LEDR Write 1 to turn red LED on, write 0 to disable.

LEDG Write 1 to turn green LED on, write 0 to disable.

Reserved Reserved positions should be written as zero for compatibility with future products.

RESET:

-	0	-	1	1	1	-	0

6.3 Serial Port Interface

6.3.1 Serial Port address space

The UART controllers are mapped into memory address space

Address Offset	accesses:
BAR2 + 0x1000..0x1008	UART 0
BAR2 + 0x1100..0x1108	UART 1

The serial port UARTs are implemented inside the FPGA and are 16550 compatible (16 bytes FIFO).

On customer request other serial port options are possible, but *not yet* implemented:

- The COM Express Typ 6 defined serial ports (Rx/TX only) can be routed to the connectors. Implementation depends on availability on the COM Express module. Sometimes such ports are available as legacy ports, sometimes as USB based ports, sometimes as custom ports, sometimes they are not available at all.
- LPC based legacy serial ports (IO address) can be implemented in FPGA if legacy ports are required for software compatibility. BIOS support for such ports can be a difficult issue however.

6.4 NVRAM

The emPC-CXR implements an integrated nvSRAM memory. This device implements 128kx8 NVRAM. The NVRAM is a fast SRAM style device, however there is no need for battery maintenance.

Address	Description
BAR5 + 0x080000..0x09FFFF	NVRAM area

Table 13: NVRAM address (128KByte NVRAM)

The NVRAM can be accessed by 8-, 16- and 32 bit operations (read and write).

If NVRAM is accessed by 16/32 bit operations, these are not atomic. In case of power down, it might happen that only parts of the 16/32 bit value are stored in the nvSRAM. Also notice that the PCI interface has buffers. Even if the write operation has been finished from CPU point of view, it might not have been saved into the memory. To make sure data has reached the memory, you need to read back the latest written content.

6.5 Digital IO

Programming the digital IO is utilized by reading/writing register in the FPGA register space.

Address Offset	access	Description
BAR5 + 0x00	-	-
BAR5 + 0x01	RW	DIGIO_OUT
BAR5 + 0x02	WO	DIGIO_IN
BAR5 + 0x03	RO	DIGIO_STAT

Table 14: Digital IO registers

DIGIO_OUT **BAR5+0x1 (byte, rw)**

7	6	5	4	3	2	1	0
write 0, read as don't care				OUT3	OUT2	OUT1	OUT0

DIGIO_IN **BAR5+0x2 (byte, ro)**

7	6	5	4	3	2	1	0
IN3	IN2	IN1	IN0	read as don't care			

IN3..0 status of the digital input line
OUT3..0 0: input voltage 0..4V
1: input voltage 9..24V

DIGIO_STATUS **BAR5+0x3 (byte, ro)**

7	6	5	4	3	2	1	0
							NO

NO 1: Normal operation.
0: Overheat condition; the output port is shutting down. This may result in cooling down the chip which sets the NO flag back to 1. If the error still exists, the chip will heat up again and the NO flag will be set to 0.

6.6 FPGA Reprogramming

An interface is provided to reprogram the SPI Flash of the FPGA.

SPI_RX **BAR0 + 0x100 (32bit, ro)**

31..0
RX_DATA

RX_DATA Data read from SPI FLASH. Data is shifted in at LSB.

SPI_TX **BAR0 + 0x104 (32bit, rw)**

31..0
TX_DATA

TX_DATA

Data to be written to SPI FLASH. Data is shifted out when SPI_TX is written and the controller is enabled (EN=1). MSB is shifted out first.

SPI_CONTROL **BAR0 + 0x108 (32bit, rw)**

31..25	24.20	19..14	14	13	12	11..1	0
Reserved	SHIFT	Reserved	WP	HOLD	CS	Reserved	EN
RESET:							
-	0	-	1	1	1	-	0

EN 1=enable SPI controller.
CS SPI FLASH chip select control (0=low)
HOLD SPI FLASH HOLD# control (0=low)
WP SPI FLASH WP# control (0=low)
SHIFT Data shift count. N+1 bits are shifted out when SPI_TX is written.
Reserved Reserved positions are undefined, and must not be considered. Write reserved bit as zero.

SPI_STATUS **BAR0 + 0x114 (32bit, ro)**

31..8	7	6..3	2	1	0
Reserved	TC	Reserved	TF	Reserved	TE
RESET:					
-	1	-	0	-	1

TE Transmitter empty flag (1=empty)
TF Transmitter full flag (1=full)
TC Transfer complete (0=busy, 1=done)
Reserved Reserved positions are undefined, and must not be considered.

7 System Control

The emPC-CXR provides some features for system control and supervision. Refer to figure 3 for the relevant components:

- The system MCU which controls the power supply and COM express module run state. Controlled either by the power supply voltage or by the control input (mid pin on the power supply connector).
- The system MCU provides an I2C slave interface on the host I2C to monitor and modify system operation.
- Access to the host I2C bus is possible by a I2C master interface which is provided by the FPGA subsystem.
- A digital temperature sensor is available and can be read via the system MCU.
- The ispPAC power sequencer which controls and monitors the internal power supplies. The integrated ADC can check any of the internal voltages and might be read via the system MCU.

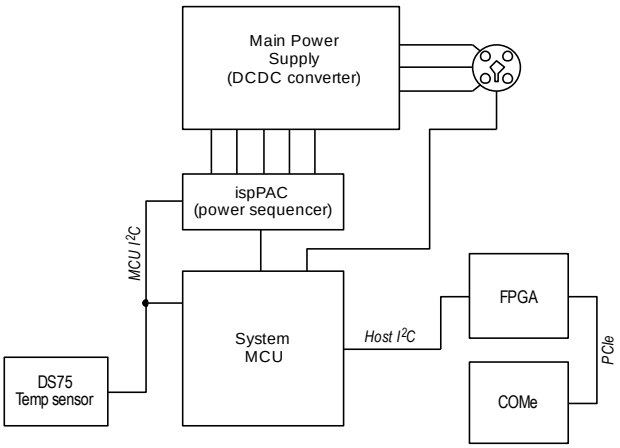


Figure 10: emPC-CXR system supervision

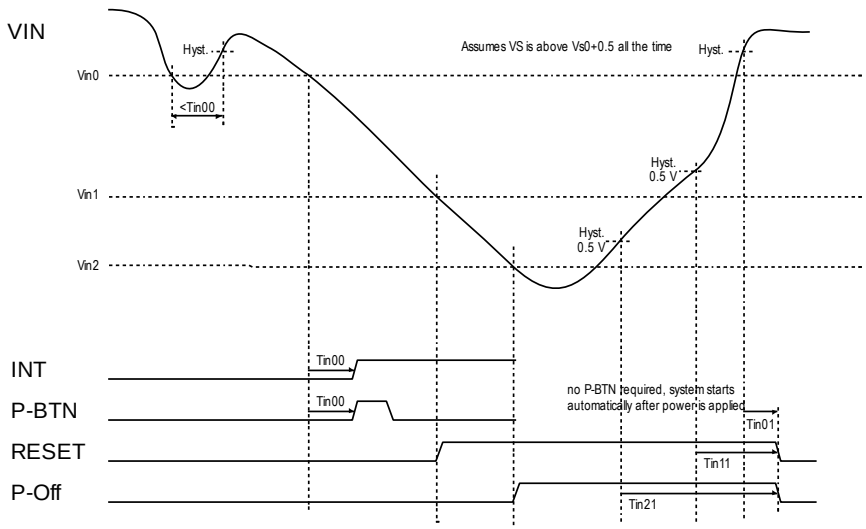


figure 11: System control by power supply voltage (VIN)

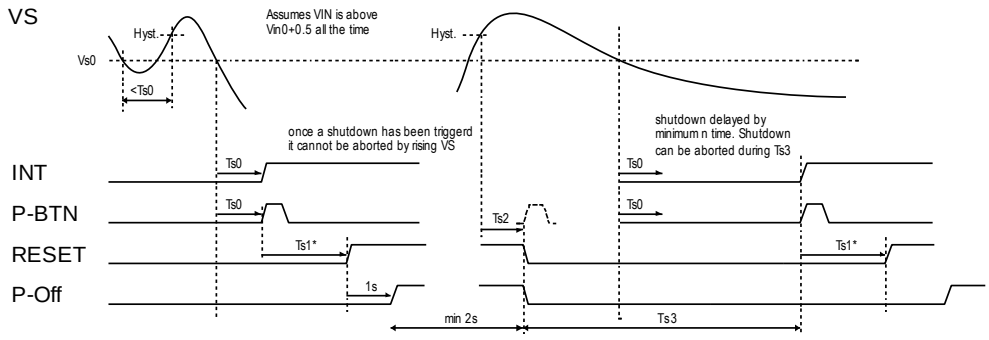


figure 12:System control by remote control input (VS)

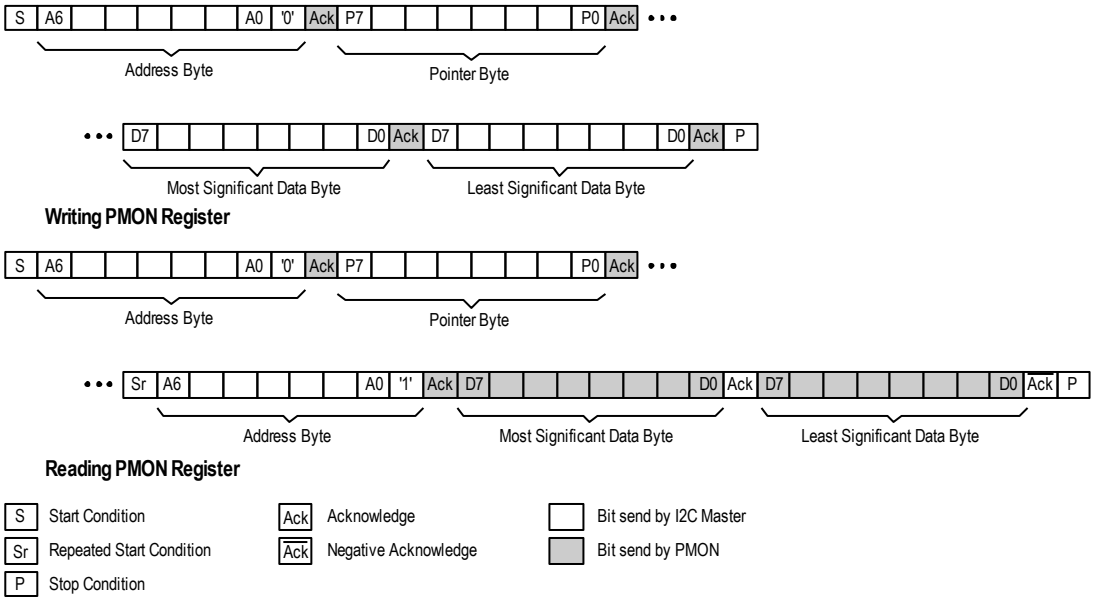


Figure 13: PMON I2C Protocols

7.1.1 I2C Address

The I2C address used by PMON is 0x60.

7.1.2 I2C Registers

All registers are 16bit wide. They are accessed indirectly by a pointer byte, which has to be written at the beginning of each transaction. Reserved registers should not be written.

Pointer	Register	EEPROM save
0x00	ID	
0x01	CONTROL	Yes
0x02	STATUS	
0x03	COMMAND	
0x04	DATA	
0x05	Reserved	
0x06	VIN_ACTUAL	
0x07	VS_ACTUAL	
0x08	VIN0	Yes
0x09	VIN1	Yes
0x0A	VIN2	Yes
0x0B	VS0	Yes
0x0C	VHYST	Yes
0x0D .. 0x0F	Reserved	
0x10	TIN00	Yes
0x11	TIN01	Yes
0x12	TIN11	Yes
0x13	TIN21	Yes
0x14	TS0	Yes
0x15	TS1	Yes
0x16	TS2	Yes
0x17	TS3	Yes
0x18	TS4	Yes
0x19..0x1f	Reserved	
0x20	TEMP	
0x21	FANCON_RDWR	

0x22	EEPROM_CTRL	
0x23..0xFF	Reserved	

Indicated register settings can be internally saved to EEPROM. These values will then be restored upon power on of PMON.

Registers that are not documented are reserved for future feature enhancement of the MCU firmware. They should not be written to avoid compatibility problems with future versions.

Following you find the description of the defined registers. All voltage related registers are stored in units of 1/100 V, all time related registers are stored in units of 10 ms (for a maximum parameter of 650s) and all temperature related registers are stored in units of 0.1 degrees Celsius.

Various parameters are visualized in figure 11 and figure 12.

ID **Pointer 0 (16bit, ro)**

15	0
PMONID	

PMONID This provides possibility to identify the PMON functionality and will be used to indicate revisions in the future.
Check for the value 0x0802 to match with this document.

CONTROL **Pointer 1 (16bit, ro)**

15	0
	EXB

RESET:

Restored from EEPROM

EXB If this bit is set, the VS input (mid contact on power connector) act as an power button input. If VS is > 5 V (typ.), the COM Express PWRBTN# signal is asserted.
If this function is activated, you should program the VS0 threshold to zero.

Reserved Reserved bits should be written as zero.

STATUS **Pointer 2 (16bit, ro)**

15	14	13	12	11	10	9	8	7		5	4	0
				WDR	BOR	EXR	POR				FSTATE	

RESET:

undefined

FSTATE The state of the PMON internal state machine.
POR Set to one if last PMON MCU reset was a power-on reset.
EXR Set to one if last PMON MCU reset was an external reset.
BOR Set to one if last PMON MCU reset was a brown-out reset.
WDR Set to one if last PMON MCU reset was a watchdog reset.

COMMAND **Pointer 3 (16bit, wo/ro)**

15	0
CMDCODE	

RESET:

0

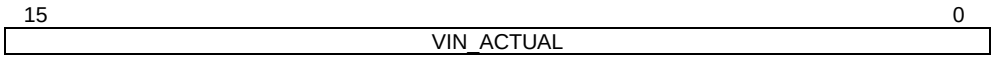
CMDCODE To trigger functions in the PMON firmware, write the corresponding command code into this register.

Once the command has completed, the register is cleared to zero by the PMON firmware.

DATA **Pointer 4 (16bit, rw)**

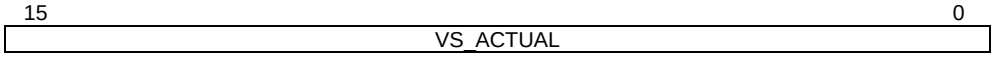
DATA Data to be supplied with the command to be executed is supplied in this register. Write to DATA before writing to COMMAND.

VIN_ACTUAL **Pointer 6 (16bit, rw)**



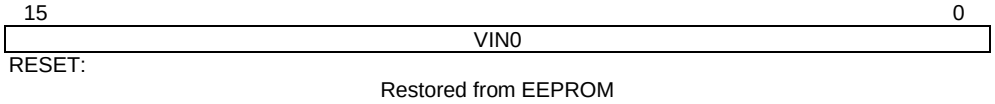
VIN_ACTUAL Voltage reading of the power supply voltage (+ contact on power connector). Reading is in units of 1/100 V, so that register value of 0x800=2048 corresponds to 20.48 V.

VS_ACTUAL **Pointer 7 (16bit, rw)**



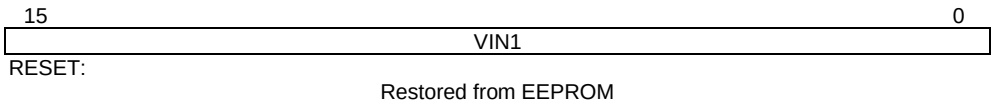
VS_ACTUAL Voltage reading of the sense voltage input (mid contact on power connector). Reading is in units of 1/100 V, so that register value of 0x800=2048 corresponds to 20.48 V.

VIN0 **Pointer 8 (16bit, rw)**



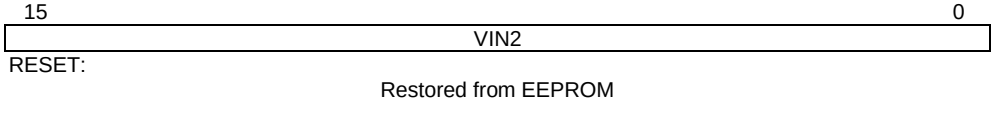
VIN0

VIN1 **Pointer 9 (16bit, rw)**



VIN1 If the power supply voltage level is below VIN1, then the system is held in reset. This state can be left if input voltage level is above VIN1+VHYST for longer than TIN11.

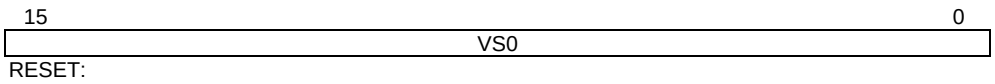
VIN2 **Pointer 10 (16bit, rw)**



VIN2 If the power supply voltage level is below VIN2, the power supply is immediately turned off. This state can be left if input voltage level is above VIN2+VHYST for longer than TIN21.
This parameter has a factory set low limit. You cannot program values below this limit. This limit might depend on the system configuration.

Generally it will be higher for a system with high power consumption to prevent operation with low voltage and high current.

VS0 **Pointer 11 (16bit, rw)**

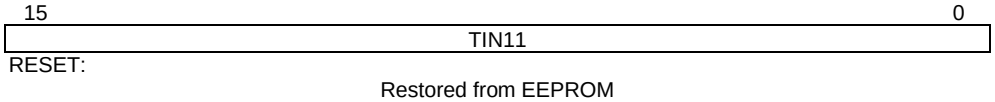


VS0 If the sense voltage level is below VS0 for a certain time, a system shutdown is triggered. When the voltage level is above VIN2+VHYST for a certain time, then a system startup is triggered. Refer to the various timing parameters for more details.
Program this register to zero to disable the sense voltage function. The sense voltage level can be read from VS_ACTUAL regardless of the VS0 setting.

VHYST **Pointer 12 (16bit, rw)**

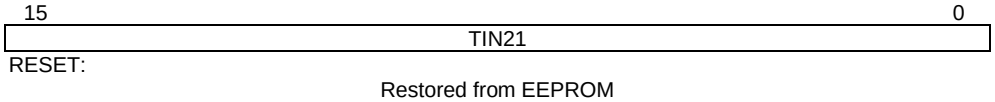
VHYST This register sets the hysteresis for the power supply and sense input signals.

TIN11 **Pointer 18 (16bit, rw)**



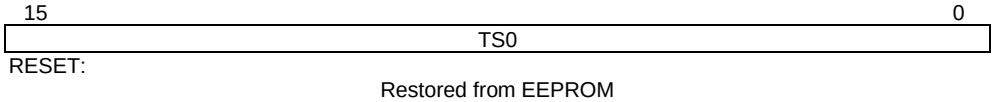
TIN11 Reset delay (see VIN1).

TIN21 **Pointer 19 (16bit, rw)**



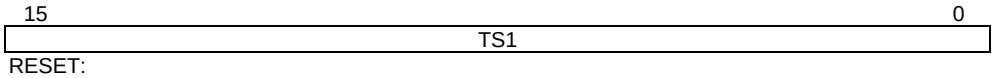
TIN21 Power good delay (see VIN2).

TS0 **Pointer 20 (16bit, rw)**



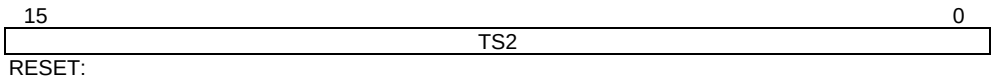
TS0 When VS is below the VS0 threshold for longer than TS0, then a system shutdown is triggerd. If VS passed VS0+VHYST before TS0 expires, then no action is taken.
However, once a system shutdown has been triggered it cannot be aborted by rising VS.

TS1 **Pointer 20 (16bit, rw)**



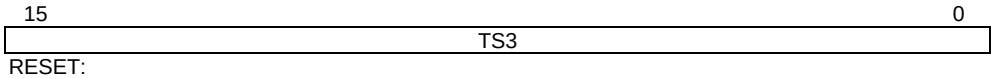
TS1 TS1 is the shutdown timeout for the system (the COM Express module). Once a shutdown has been triggered, the PMON firmware waits for the system to shut down (monitored by COM Express SUS_S3 signal). If a shutdown has not been detected after TS1 expires, then a system reset is applied and power is turned off one second later.

TS2 **Pointer 21 (16bit, rw)**



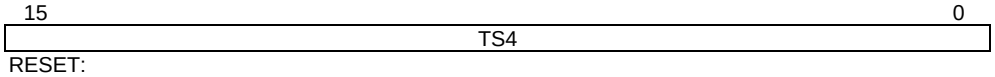
TS2 The system is off (and a minimum off time of 2 seconds has elapsed) and VS is > VS0+VHYST for longer than TS2, then the system is turned on. The power supply is turned on, and if the COM Express module does not start automatically, a single power button event is generated to force turn on.

TS3 **Pointer 22 (16bit, rw)**



TS3 A system shutdown is inhibited until the system is running for more than the time programmed by TS3. This can be used to prevent a shutdown during operating system bootup phase, when the time set by TS0 might not be enough to perform a proper shutdown.

TS4 **Pointer 23 (16bit, rw)**



TS4 Do not write to this register.

TEMP **Pointer 32 (16bit, ro)**

TEMP System temperature sensor readout. Temperature data is read as two's complement data in units of 1/10 degrees Celsius.

Register reading	Temperature/deg. C
0b0000001001010000	25.0
0b0000000000001010	1.0
0b0000000000000000	0.0
0b1111111111110110	-1.0

0b1000000000000000	Sensor error

7.1.3 Command Codes

This section lists the command codes that are accepted by the PMON firmware. Undocumented command codes should not be issued.

<table>
<tr><th>CMD code</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>IDLE</td><td>When read, this command code indicates idle state.</td></tr>
<tr><td>1</td><td>SAVE_EEP</td><td>Save all parameters that are indicated as “EEPROM saved” into the PMON MCUs internal EEPROM. This makes changes permanent.
Before writing, some simple sanity checks are made. E.g. you cannot save a voltage threshold that is higher than the supported operating value.
No checks are made on the timing parameters.</td></tr>
<tr><td>2</td><td>RESET_ERR</td><td>Reset the PMON MCU reset information in the STATUS register.</td></tr>
<tr><td>9</td><td>PACADCREAD</td><td>Read ADC data from the ispPAC chip. The channel is selected by the DATA register.
<table>
<tr><th>Channel</th><th>Voltage Rail</th><th>Factor</th></tr>
<tr><td>0</td><td>Vin</td><td>7.8</td></tr>
<tr><td>1</td><td>+12V</td><td>3</td></tr>
<tr><td>2</td><td>N/A</td><td>-</td></tr>
<tr><td>3</td><td>+5V</td><td>1</td></tr>
<tr><td>4</td><td>+3.3V</td><td>1</td></tr>
<tr><td>5</td><td>+1.2V</td><td>1</td></tr>
<tr><td>6</td><td>Vin-A</td><td>8.8</td></tr>
<tr><td>7</td><td>Vin-B</td><td>8.8</td></tr>
<tr><td>8</td><td>N/A</td><td>-</td></tr>
<tr><td>9</td><td>N/A</td><td>-</td></tr>
</table>
The returned value is a correct ADC value if bit 0 of the DATA register is 1.
To convert to a voltage value use the following formula:
Voltage/mV = ((DATA>>4)&0xfff) * 2 * factor
Where factor is taken from the table above.

Vin-A and Vin-B channels allow to monitor both power supply inputs independently, to allow identify broken down power supplies. Accuracy is not very high for these channels.</td></tr>
</table>

8 Appendices

8.1 Technical Data

Standard Configuration:

Processing Core	
CPU	**C-1047UE**: Intel Celeron 1047UE, 2 x 1.4 GHz, 2 MB cache **i7-3517UE**: Intel i7 3517UE, 2 x 1.7 / 2.8 GHz, 4 MB Cache See http://ark.intel.com/ for more details about the CPUs
Chipset	Intel® 7 Series Platform Controller Hub
COMexpress Module	GE bCOM6-L1400
Memory	
Main Memory	4 GB DDR3 1600MT/s
nvSRAM	128 kB nvSRAM
Storage	
mSATA	1 x with SATA interface
Video	
Controller	Chipset graphics
Memory	Shared with main memory
Interface	VGA, up to 2048x1536
External Interfaces	
Video	1 x VGA
Ethernet	1 x 10/100/1000 Mbit/s Ethernet (LAN1: Intel 82579) 1 x 10/100/1000 Mbit/s Ethernet (LAN2: Intel i210)
USB	2 x USB2.0
CAN	2 x 9 pin D-Sub, ISO/DIS 11898-2, isolated from logic, switchable termination resistor, SJA1000 controller Rated isolation voltage 60V to shield and internal logic Isolation barrier tested 800VDC for 1 min,
Digital IO	4 x digital In/Out, isolated from logic, 10..34 V external power supply, 0.5 A output current per output, 1 A output current for all ports in total. Rated isolation voltage 30V to shield and internal logic Isolation barrier tested 800VDC for 1 min
Indicators and Switches	
Remote Control	1 x Signal input on power connector for pushbutton or run-control function
Status LEDs	1 x Green LED for power supply status
System	
Housing	anodized aluminium
Battery	BR 2032, for real time clock
Battery Lifetime	3.5 years
System controller	Temperature sensing and power supply management (accessible via FPGA I2C bus)
Watchdog	Yes, implemented by COM Express module
FPGA	Spartan 6 LX25T, PCI express interface to baseboard IOs

Power Requirements

Power Supply	DC power, 9 .. 34 V (lower limit with adjustable UVL)
Inrush Current (max)	Not controlled
Power Dissipation	Without external load or expansion cards **C-1047UE**: 33 W (max) **i7-3517UE**: 35 W (max)

External Load Capabilities

+5V (USB)	Max. 0.5 A per USB port

Environmental Specifications

Ambient Operating Temperature	**C-1047UE**: -40..+70°C when installed in restricted access location, -40..+60°C in all other locations[1)] **i7-3517UE**: -40..+70°C when installed in restricted access location, -40..+60°C in all other locations[1)] at sea level, derating of 1 °C per 300 m above sea level to a maximum of 2000 m.
Storage Temperature	-40..+85 °C [2)]
Humidity	5%..95% r.H., non condensing
Protection Class	IP67 (all connectors mounted)
EMC	EN 55011 Class A, EN 50155

Physical Dimensions

Size	Not including connectors (WxHxD) 266 x 196 x 87,75 mm
Unit Weight	5,2 kg
Packaged Weight	6,2 kg

Notes:

1) This restriction limits the housing temperature in locations where it is possible that the product surface is touched.
2) Storage at high temperatures will reduce battery life

8.2 References

These references direct you to manuals and specifications that you might need to know when you attempt to program the product. Most of the documents can be downloaded from the Internet. Look for the WWW servers of the component/chip manufacturers.

[1]
[2]
[3]

WWW-References

Janz Tec AG	www.janztec.com
Intel Corporation	www.intel.com

8.3 M12 Connector Ratings

For informational purposes here the isolation ratings of the M12 Connectors (as specified by Phoenix Contact):

Type	Rated Voltage	Rated Surge Voltage (Pin to Pin)	Rated Surge Voltage (Pin to Shield)	Rated Current (40 °C)
M12-5	60 V	1500 V	1500 V	4 A
M12-8	30 V	800 V	800 V	2 A
M12-T	60 V	1500 V	1500 V	12 A
M12-X	48 V	1500 V	2230 V	0.5 A

Check that mating connectors are rated equal or higher.

8.4 Dimensions

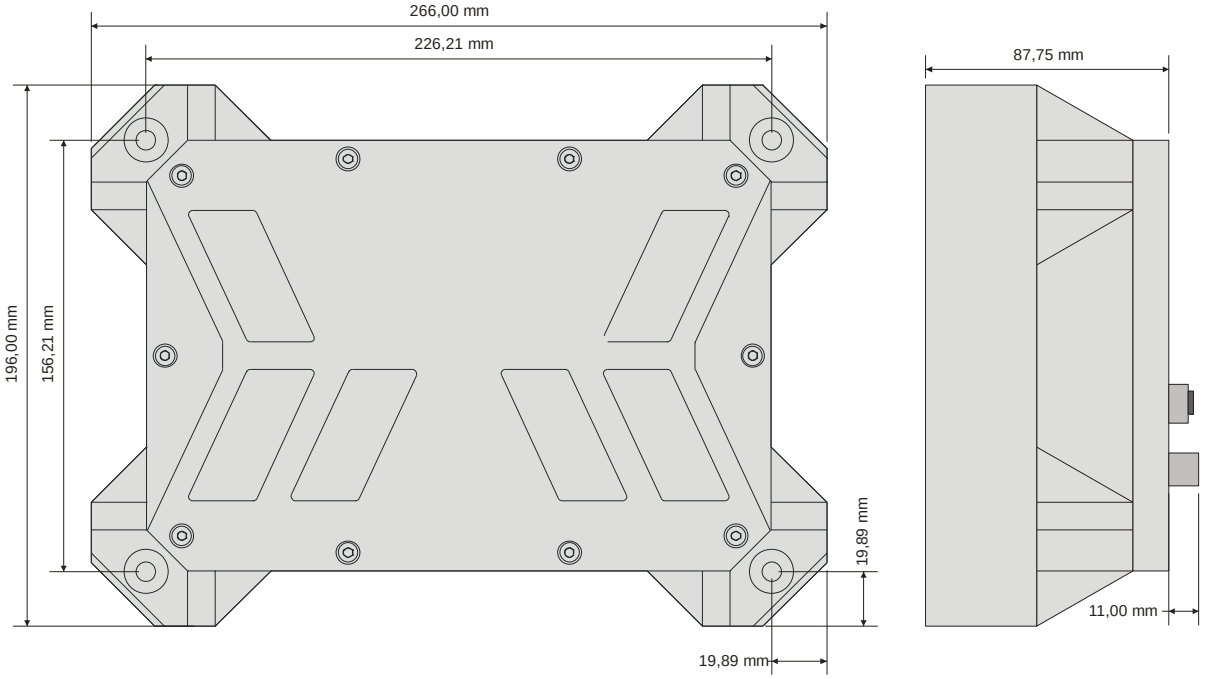


figure 14: housing dimensions

8.5 Product History

TBD

8.6 Manual History

Version	Release Date	Name	Changes
V1.0	2015-01-15	As	• Created for version 1.0
V1.1	2015-06-23	As	• Added more details • Added Celeron CPU variant • Modified M12-8 IO connector pinout to match the register description (no functional change) • Power supply connector input KL2 was renamed VS
V1.2	2015-11-25	AS	• Added Celeron Power and Battery Lifetime • Added Torque for top cover screws • Fixed some doc errors • Fixed system description (page 2)
V1.3	2016-01-18	As	• Incorporated some hints from TÜV testing.
V1.4	2018-11-14	As	• Changed image in maintenance section