EmCORE-i2709

3.5” Compact Board

User’s Manual

Version 1.2

2011.07

This page is intentionally left blank.

Contents

This page is intentionally left blank.

Chapter 1

Introduction

1.1 Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

1.2 Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions : (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl

ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

1.3 About This User's Manual

This user's manual provides general information and installation instructions about the product. This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. please consult your vendor before further handling.

1.4 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

1.5 Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

1.6 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw

E-mail:info@arbor.com.tw

1.7 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.8 Packing List

Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

1 x EmCORE-i2709 3.5” Compact Board with heat sink

1 x Driver CD
1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

1.9 Ordering Information

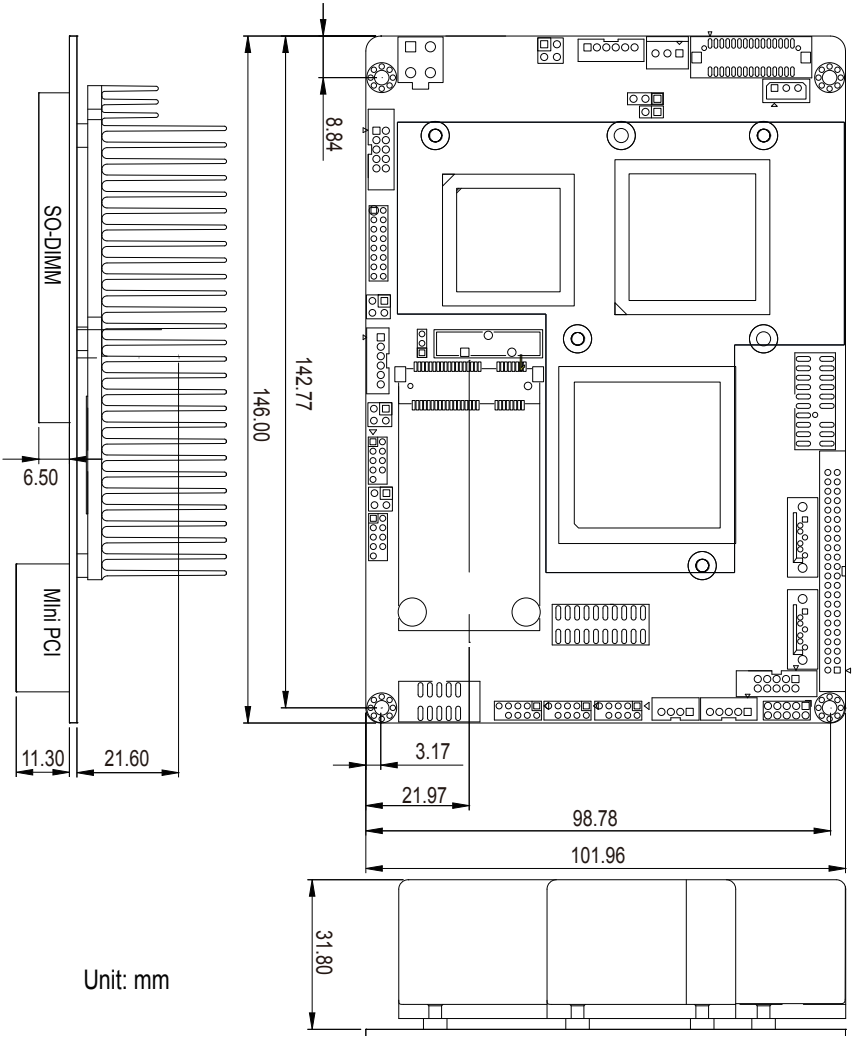
EmCORE-i2709	Intel Atom™ N270 1.6GHz 3.5” Compact Board
FCDB-1293	4 x COM ports & digital I/O daughter board
CBK-11-2709-00	Cable Kit 1 x Audio Cable 2 x COM Port Cables 1 x IDE Cable 1 x KB & MS Cable 2 x LAN Cables 1 x LPT to FDD Cable 1 x Parallel Port Cable 2 x SATA Cables 1 x TV-out Cable 3 x USB Cables 1 x VGA Cable

1.10 Specifications

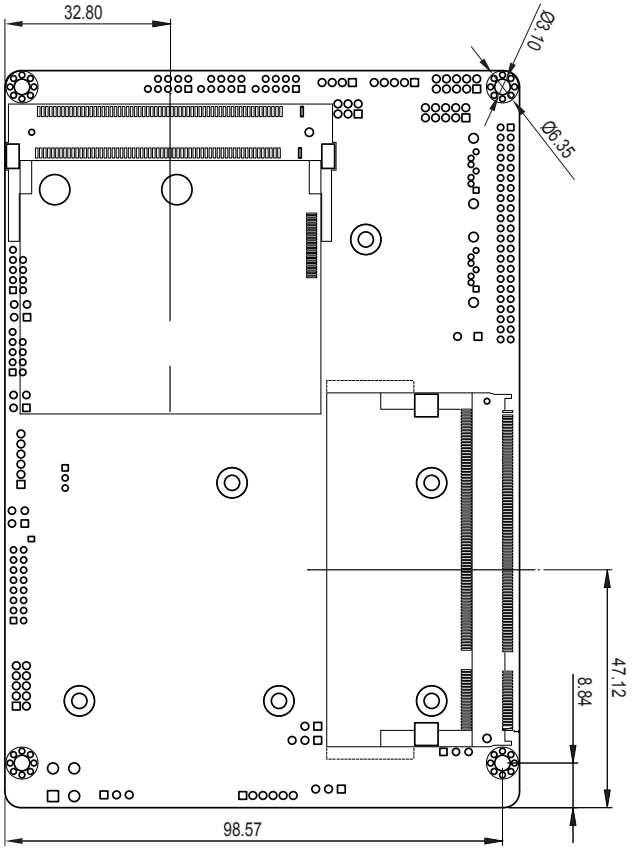
Form Factor	3.5” Compact Board
CPU	Intel® Atom™ N270 CPU 1.6GHz with 533MHz FSB
Chipset	Intel® 945GSE + Intel® ICH7M
System Memory	1 x 200-pin SO-DIMM Socket Up to 2GB DDR2 533MHz SDRAM (Bottom side)
VGA/ LCD Controller	Integrated Intel Graphics Media Accelerator 950, Dual Channels 24-bit LVDS
Ethernet	2 x Realtek 8111 PCIe Gigabit Ethernet controllers
I/O Chips	Winbond W83627HG
BIOS	AMI PnP Flash BIOS
Audio	Realtek ALC655 AC97 Audio CODEC, MIC-in/ Line-In/ Line-Out
Storage	2 x Serial ATA 150MB/s HDD transfer rate 1 x IDE Ultra ATA 33, support 2 IDE devices 1 x Floppy connector share with LPT port
Serial Port	2 x COM ports (COM1: RS-232, COM2: RS-232/422/485 selectable)
Parallel Port	1 x LPT Port (SPP/EPP/ECP mode selectable)
KBMS	One 6-pin wafer connector (PS/2 interface Keyboard and Mouse via cable)
Universal Serial Bus	6 x USB 2.0 ports
Digital I/O	8-bit programmable Digital Input/Output
Expansion Interface	1 x Mini-Card Slot 1 x Mini PCI Socket (Bottom side)
Operation Temp.	-20°C ~ 70°C (-4°F ~ 158°F)
Watchdog Timer	1~255 levels Reset
Dimension (L x W)	146 x 102 mm (5.7 ” x 4.0 ”)

1.11 Board Dimensions

Top View

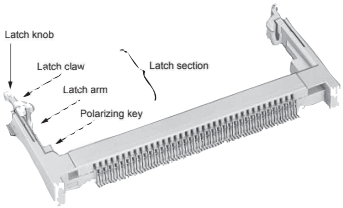


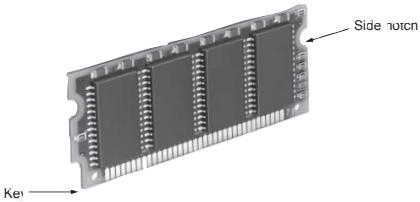
Bottom View



Unit: mm

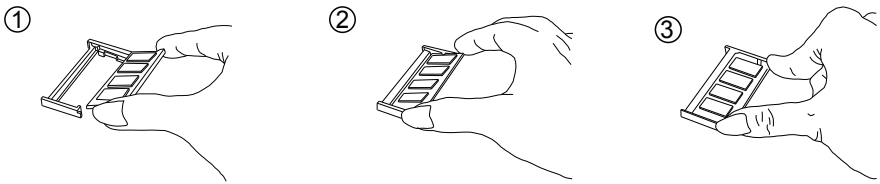
1.12 Installing the Memory





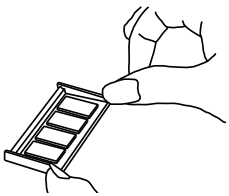
To install the Memory module, locate the Memory SO-DIMM slot on the board and perform as below:

1. Adjust the socket polarizing key and the board key to the same direction.
2. Insert the board obliquely. Moreover, lay the board in parallel to the opening at angle of 20^{o} to 30^{o}, and softly insert the board so as to hit the socket bottom. Stopping insertion halfway will result in improper insertion.
3. Applying the board side notch in parallel to the socket bottom so that the board position cannot be displaced, press the board side notch up, and fix it to the latch portion at both socket edges. Press the board side notch, and release the notch with a snap “click” tone, if the printed board exceeds the latch claw head.



Procedures for board extraction

Apply the thumb nail to the latch knob at both socket edges. Forcibly widen the latch knobs to right and left ways, and release the latch. Then draw the board out along an angle where the board is raised.

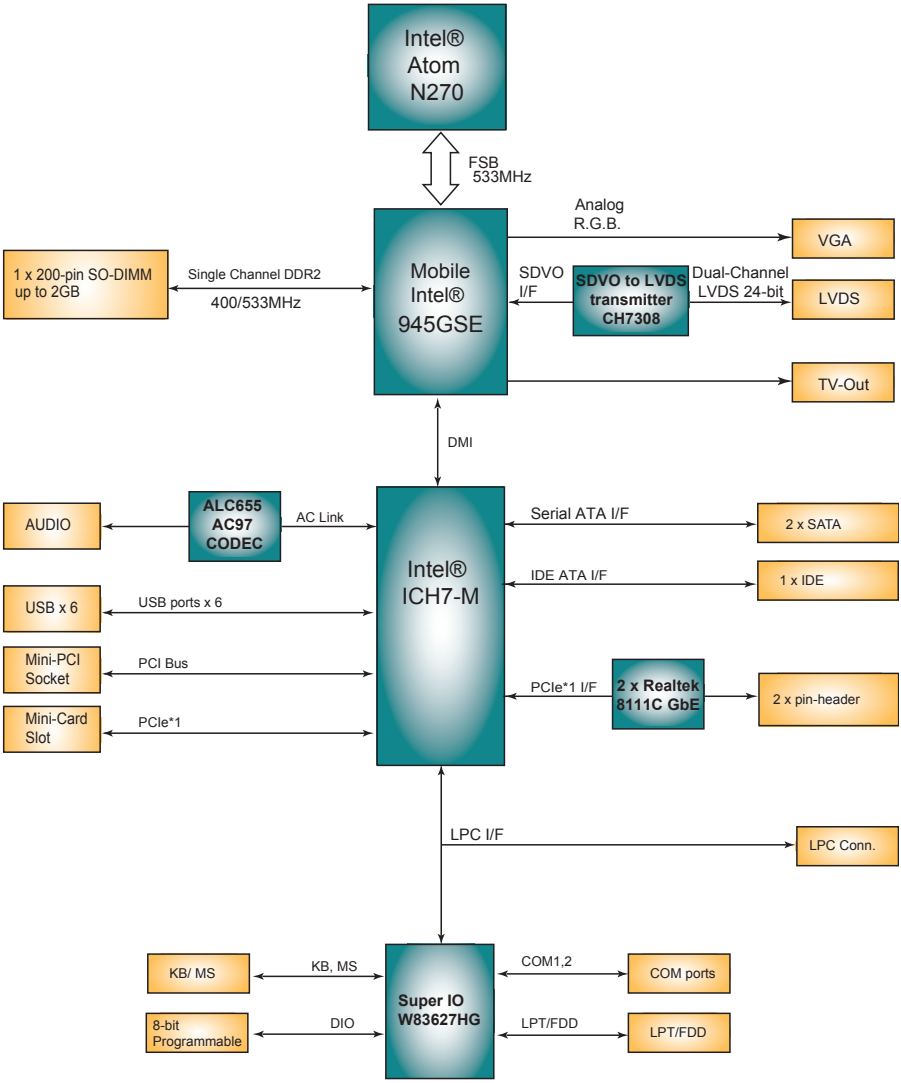


This page is intentionally left blank.

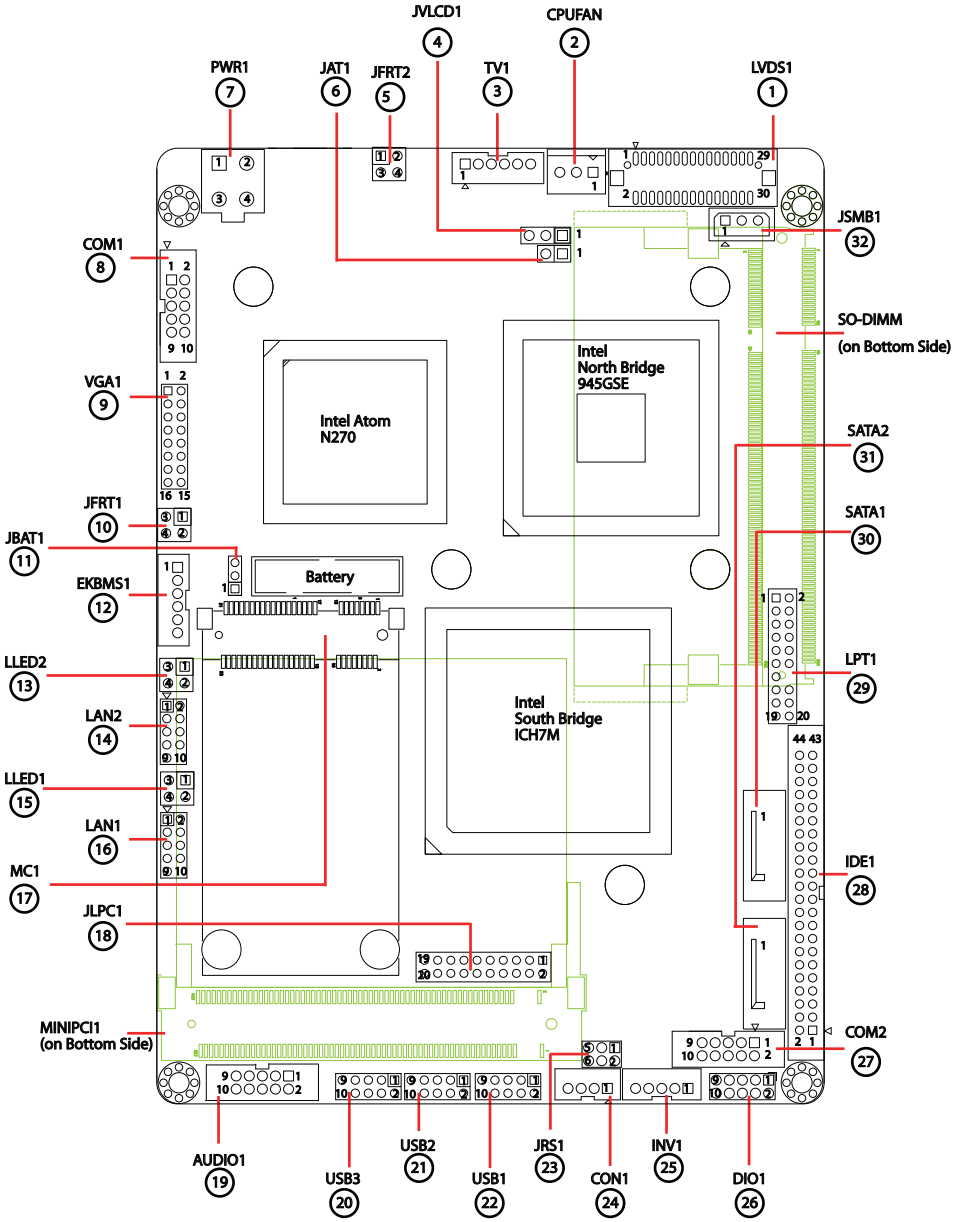
Chapter 2

Installation

2.1 Block Diagram



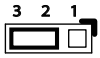
2.2 Jumpers and Connectors

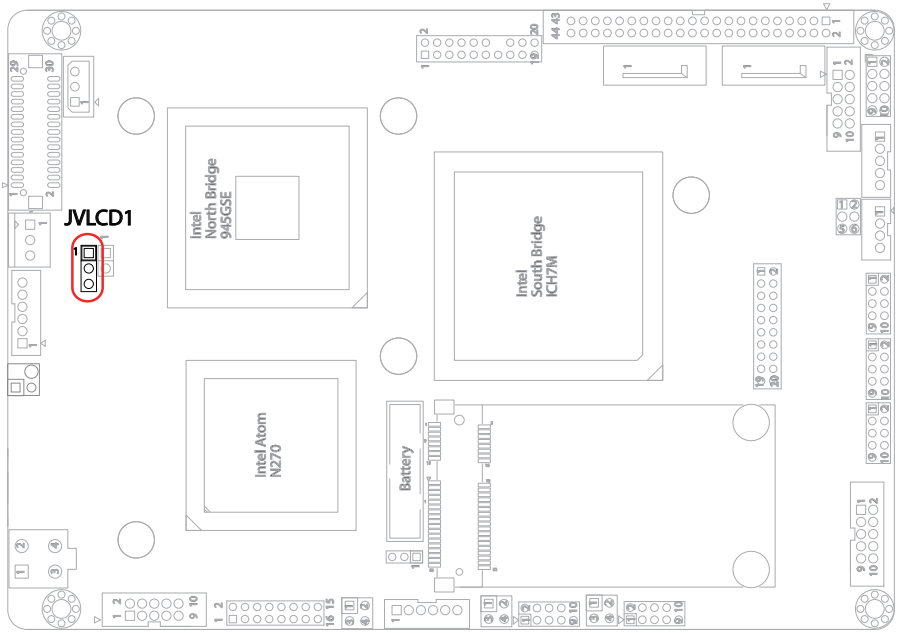


Jumpers

JVLCD1: LCD Panel Voltage Selection (4)

The voltage of LCD panel could be selected by JVLCD1 in +5V or +3.3V.
Connector type: 2.54 mm pitch 1x3-pin headers

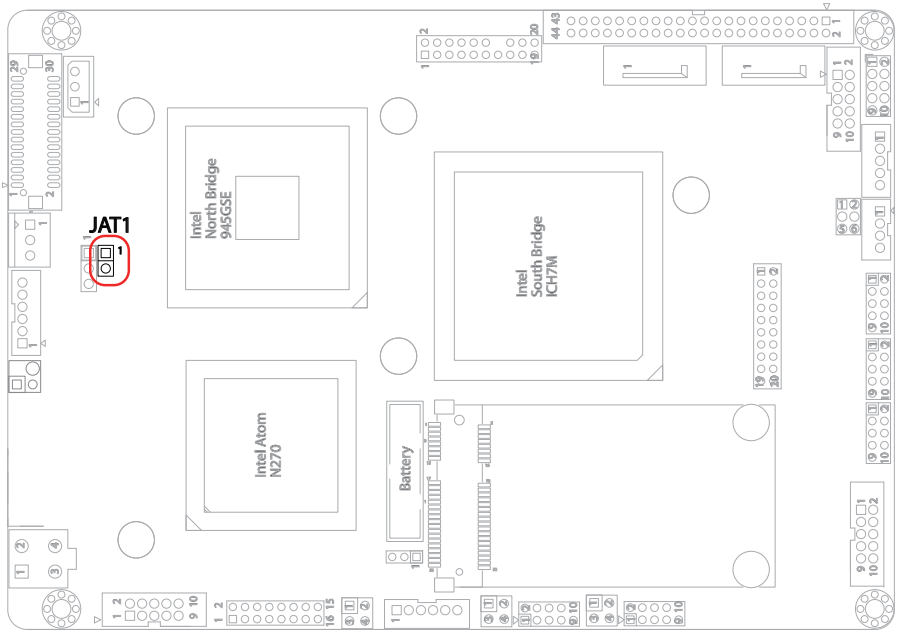
Pin	Voltage	
1-2	+5V	
2-3	+3.3V (Default)	



JAT1: AT/ATX Power Mode Selection (6)

The power mode jumper selects the power mode for the system.
Connector type: 2.54mm pitch 1x2 pin headers.

Pin 1-2	Mode	
Short	AT Mode	1 2
Open	ATX Mode (Default)	1 2



Note:
To activate the ATX power mode, you must turn on the power button switch first (the connector for power button swtich is located in JFRT1).

JBAT1: Clear CMOS Setting (11)

If the board refuses to boot due to inappropriate CMOS settings here is how to proceed to clear (reset) the CMOS to its default values.
Connector type: 2.00mm pitch 1x3-pin headers

Pin	Mode	
1-2	Keep CMOS (Default)	
2-3	Clear CMOS	

You may need to clear the CMOS if your system cannot boot up because you forgot your password, the CPU clock setup is incorrect, or the CMOS settings need to be reset to default values after the system BIOS has been updated.
Refer to the following solutions to reset your CMOS setting:

Solution A:

1. Power off the system and disconnect the power cable.
2. Place a shunt to short pin 2 and pin 3 of JBAT1 for five seconds.
3. Place the shunt back to pin 1 and pin 2 of JBAT1.
4. Power on the system.

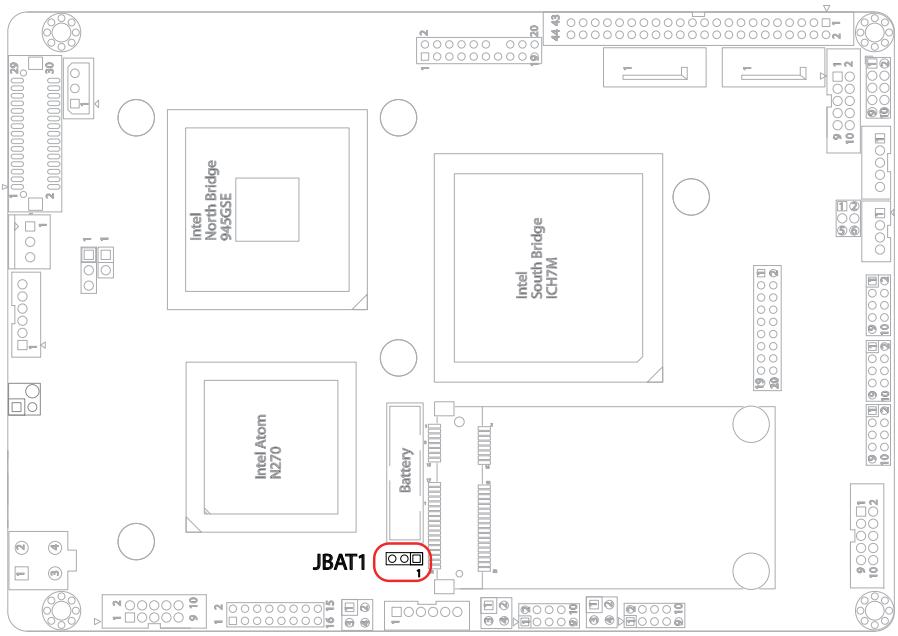
Solution B:

If the CPU Clock setup is incorrect, you may not be able to boot up. In this case, follow these instructions:

1. Turn the system off, then on again. The CPU will automatically boot up using standard parameters.
2. As the system boots, enter BIOS and set up the CPU clock.

Note:

If you are unable to enter BIOS setup, turn the system on and off a few times.

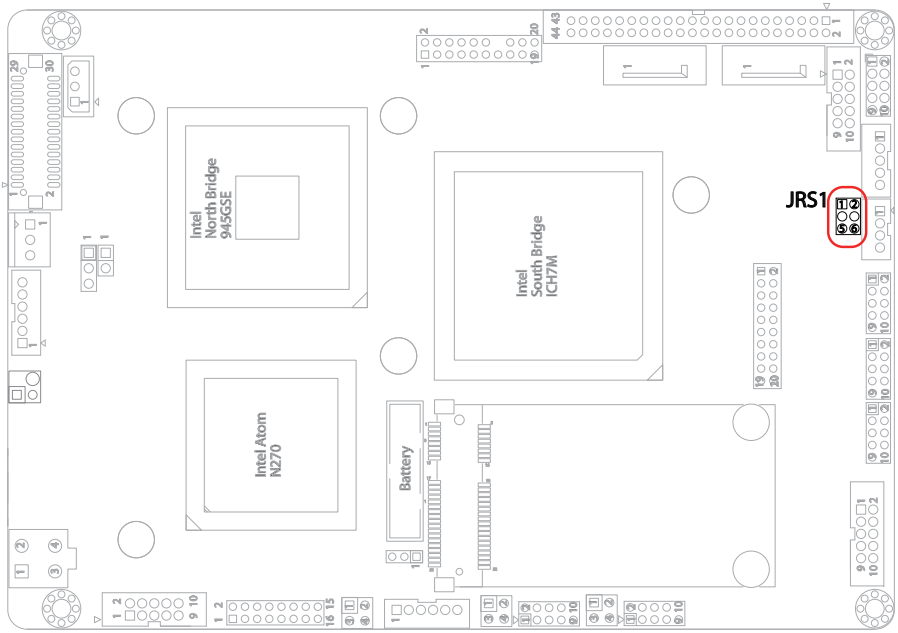

Intel
North Bridge
945GSE
Intel
South Bridge
ICH7M
Intel Atom
N270
Battery
JBAT1

JRS1: COM2 RS-232/422/485 Mode Selection (23)

The onboard COM2 port can be configured to operate in RS-422 or RS-485 modes. RS-422 modes differ in the way RX/TX is being handled. Jumper JRS1 switches between RS-232 or RS-422/485 mode. All RS-232/422/482 modes are available on COM2. COM2 can be configured to operate in RS-232, RS-422 or RS-485 mode.

Connector type: 2.00mm pitch 2x3-pin headers.

Mode	RS-232 (Default)	RS-422	RS-485
1-2	Short	Open	Open
3-4	Open	Short	Open
5-6	Open	Open	Short
			

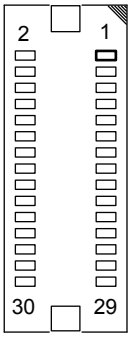


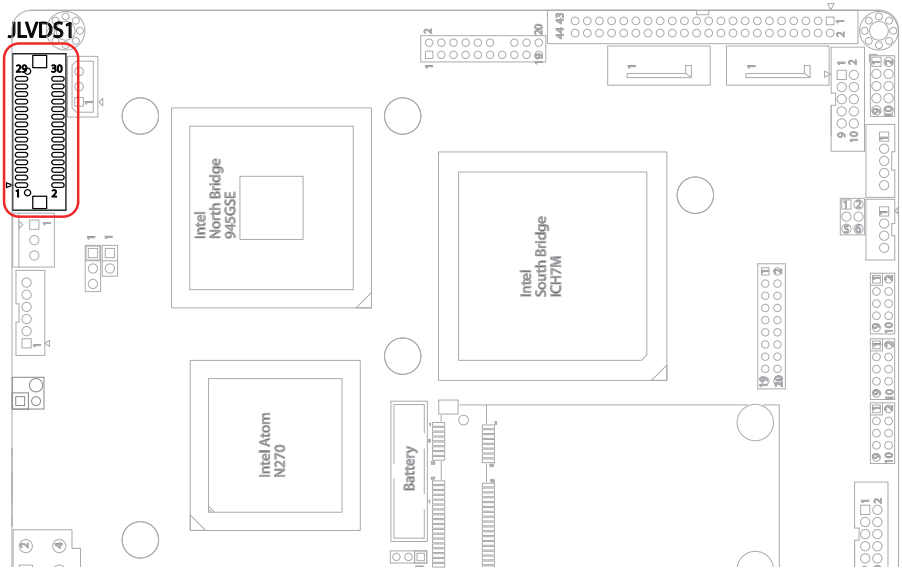
Connectors

LVDS1: LVDS LCD Connector (1)

The LVDS connector supports 24-bit dual channels LVDS.
VDD could be selected by JVLCD1 in +5V or +3.3V.
Connector type: DF-13-30DP-1.25V

Pin	Description	Pin	Description
2	VDD	1	VDD
4	TX2CLK+	3	TX1CLK+
6	TX2CLK-	5	TX1CLK-
8	GND	7	GND
10	TX2D0+	9	TX1D0+
12	TX2D0-	11	TX1D0-
14	GND	13	GND
16	TX2D1+	15	TX1D1+
18	TX2D1-	17	TX1D1-
20	GND	19	GND
22	TX2D2+	21	TX1D2+
24	TX2D2-	23	TX1D2-
26	GND	25	GND
28	TX2D3+	27	TX1D3+
30	TX2D3-	29	TX1D3-

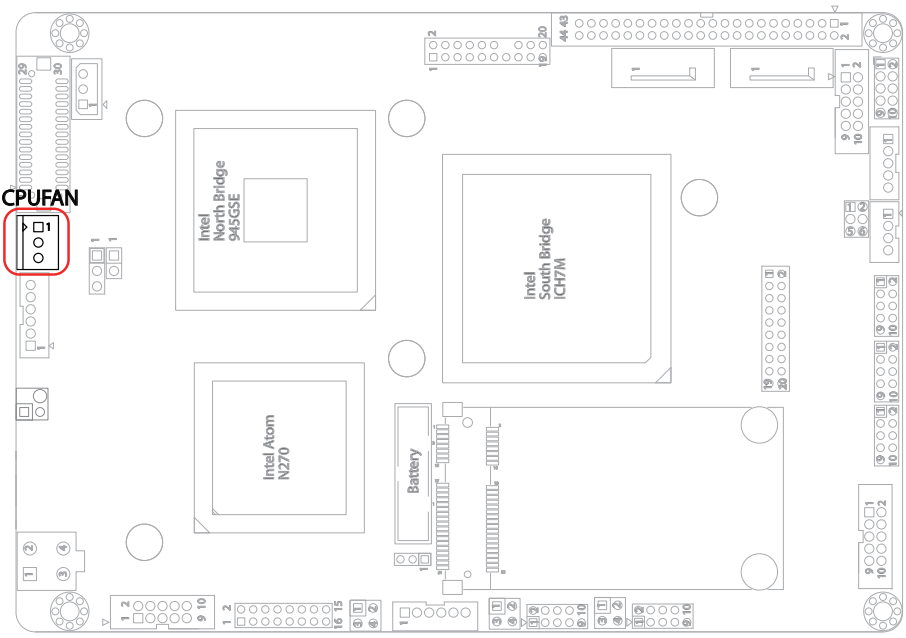




CPUFAN: Fan Power Connector (2)

CPUFAN is a 3-pin headers for the CPU fan. The fan must be a +12V fan.

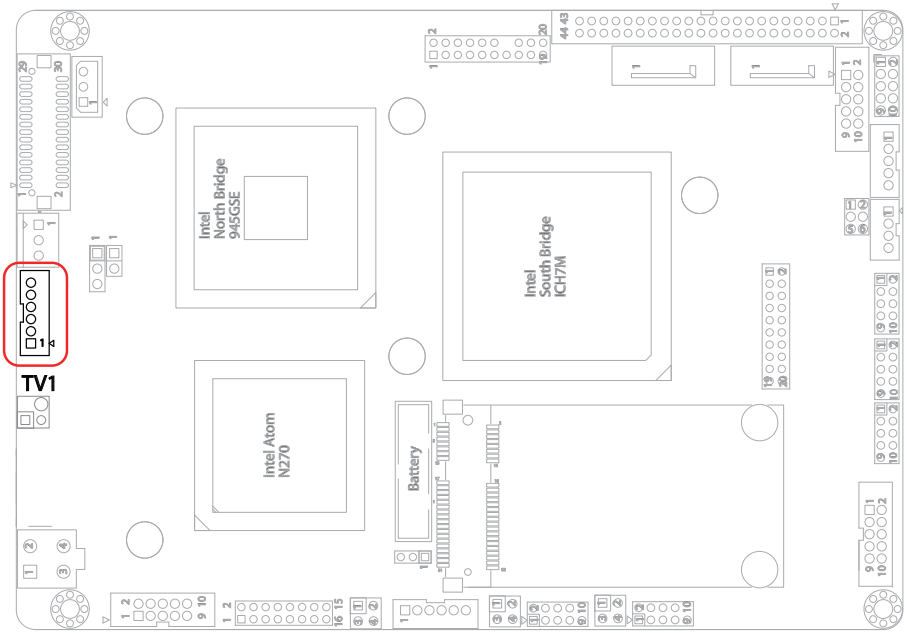
Pin	Description
1	GND
2	+12V
3	FAN_Detect



TV1: TV-out Connector (3)

The TV out connector is for output to a television.
Connector type: 2.00mm pitch 1x6-pin box wafer connector

Composite Video			
1	CVBS	2	GND
3	Unused	4	GND
5	Unused	6	GND
S-Video			
1	Unused	2	GND
3	Luminance	4	GND
5	Chrominance	6	GND

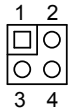


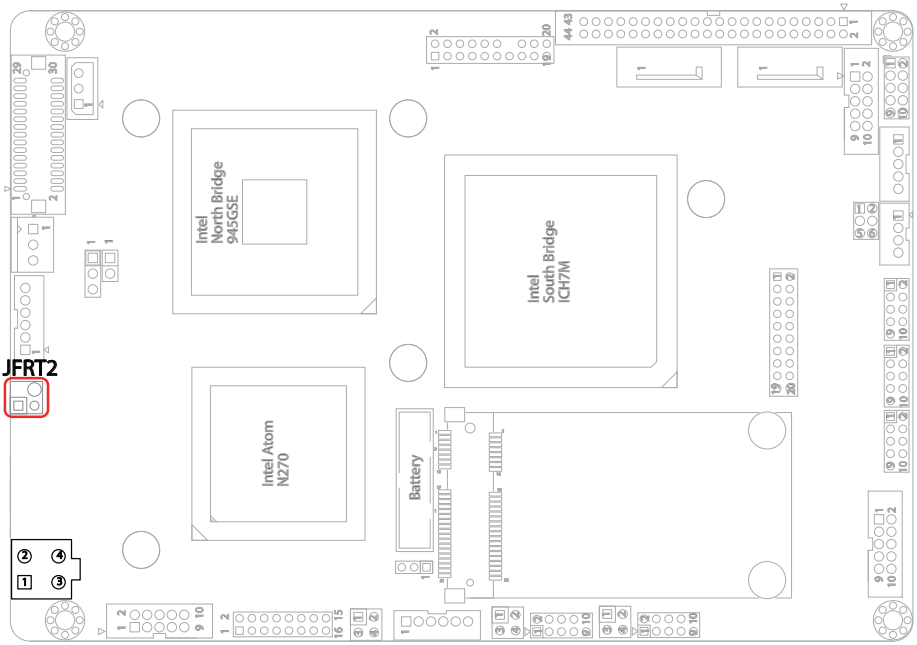
JFRT2: LED Indicators (5)

This connector provides signals for LED indicators presenting the status of the system.

Connector type: 2.54 mm pitch 2x2-pin headers

Pin	Description	Pin	Description
1	PWRLED+	2	PWRLED-
3	HDDLED+	4	HDDLED-

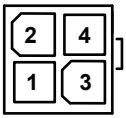


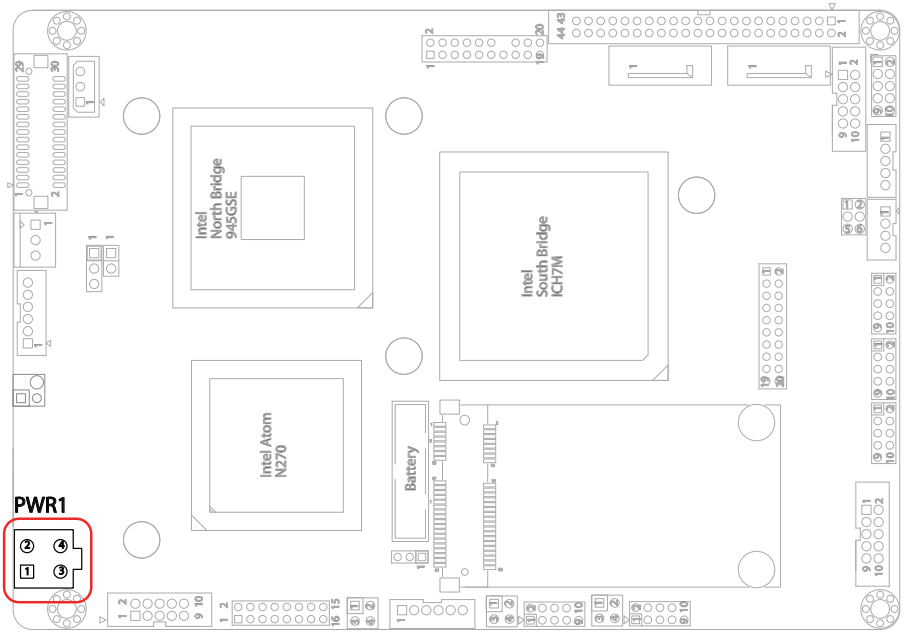


PWR1: +12V Connector (7)

PWR1 supplies CPU operation at +12V (Vcore).

Pin	Description	Pin	Description
2	GND	4	+12V
1	GND	3	+12V

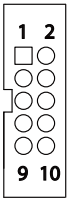


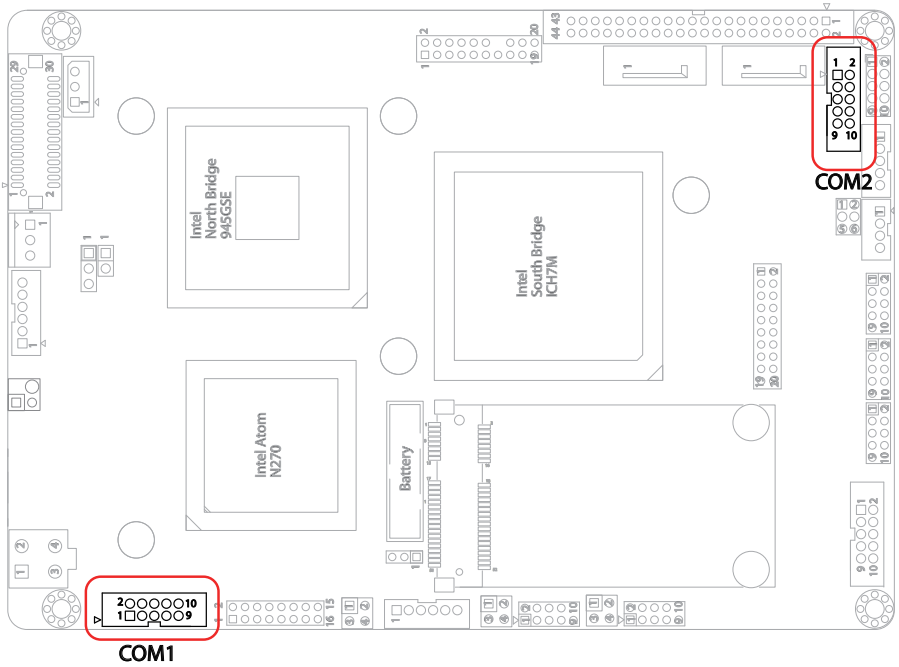


COM1~2: RS-232 Connectors (8, 27)

Connector type: 2.00mm pitch 2x5-pin box headers.

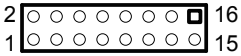
Pin	Description	Pin	Description
1	DCD#	2	RXD
3	TXD	4	DTR#
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	N/C



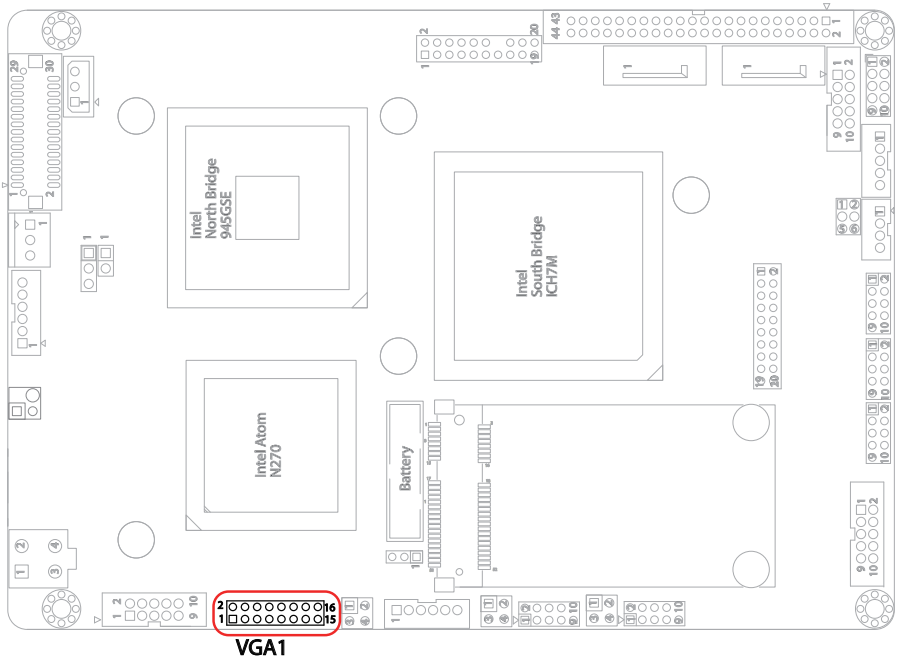


VGA1: Analog RGB Connector (9)

Connector type: 2.00mm pitch 2x8-pin headers.



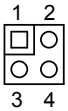
Pin	Description	Pin	Description
1	RED	2	GREEN
3	BLUE	4	N/C
5	Analog RGB_GND	6	Analog RGB_GND
7	Analog RGB_GND	8	Analog RGB_GND
9	Analog RGB_VCC	10	Analog RGB_Detect
11	N/C	12	DDC_DATA
13	HSYNC	14	VSYNC
15	DDC_CLOCK	16	N/C



JFRT1: Switch (10)

It provides connectors for system indicators that provides light indication of the computer activities and switches to change the computer status.
Connector type: 2.54 mm pitch 2x2-pin headers

Pin	Description	Pin	Description
1	PWRBTN+	2	PWRBTN-
3	RESET+	4	RESET-

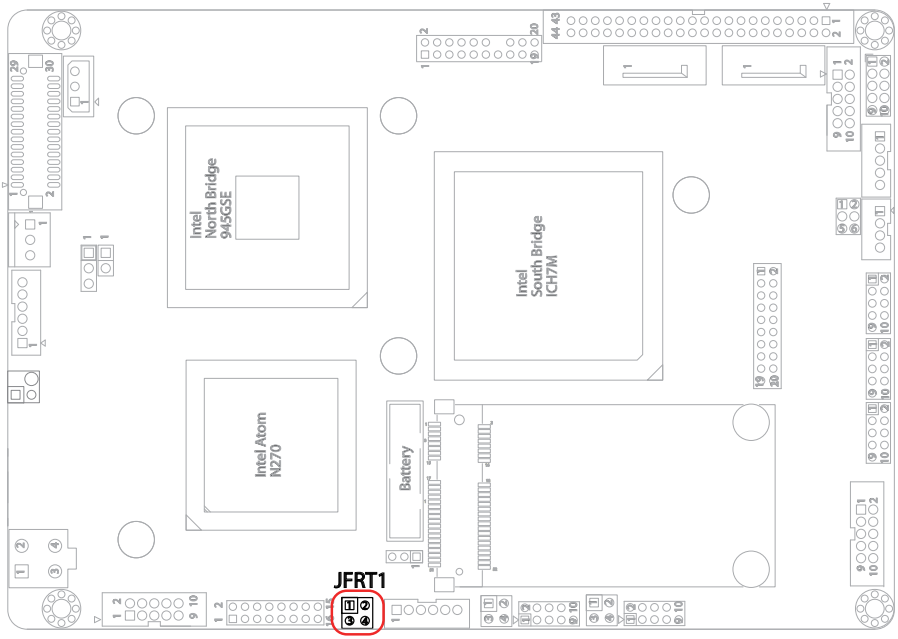


PWRBTN: ATX soft power switch, pin 1-2.

This 2-pin connector connects to the case-mounted Power button.

RES: Reset Button, pin 3-4.

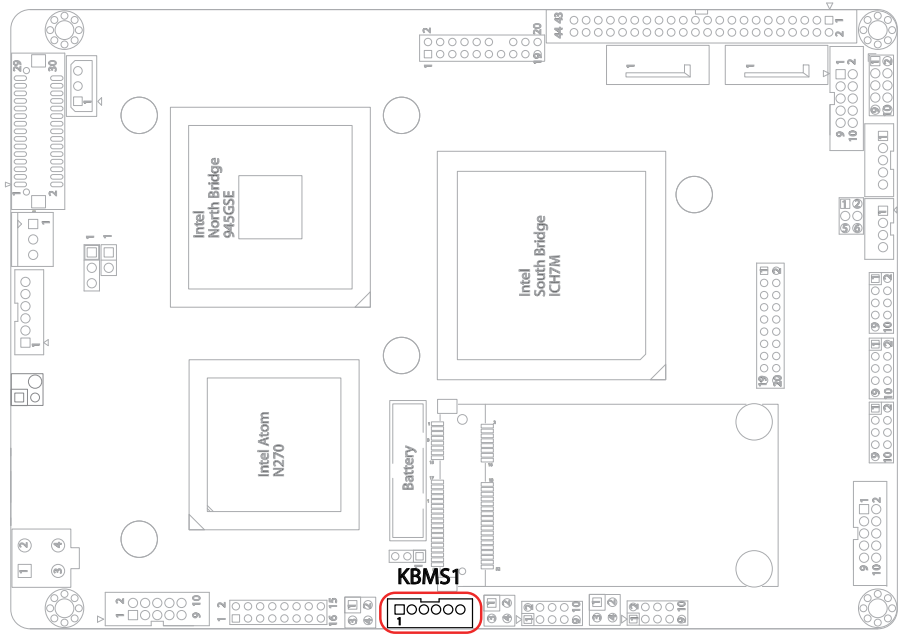
This 2-pin connector connects to the case-mounted reset switch and is used to reboot the system.



EKBMS1: Keyboard & Mouse Connector (12)

Connector Type: 2.0mm pitch 1x6-pin box wafer connector

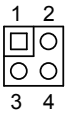
Pin	Description
1	KB_DATA
2	GND
3	MS_DATA
4	KB_CLK
5	KB_VCC
6	MS_CLK

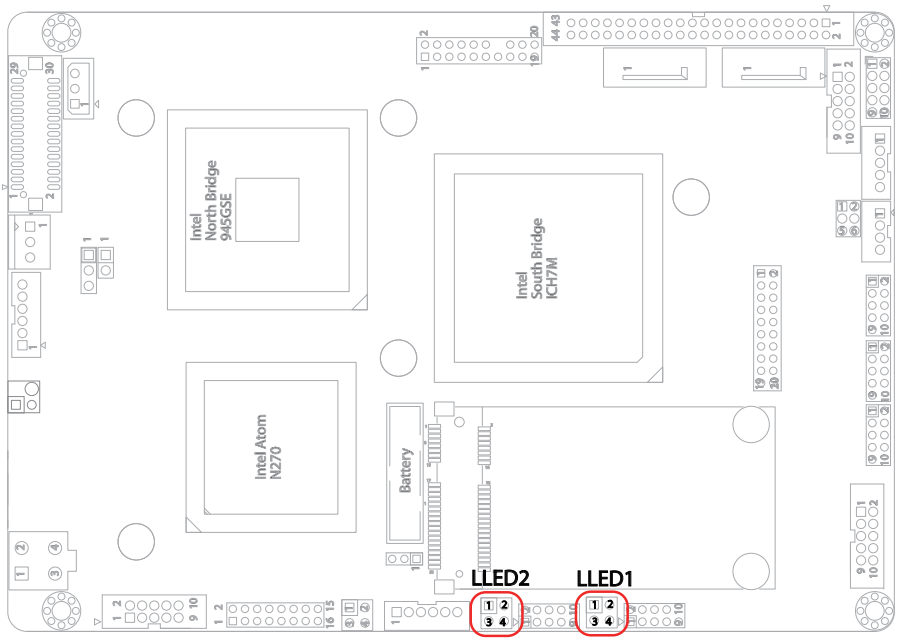


LLED1~2: LAN1/ LAN2 LED Indicators (15, 13)

Connector type: 2.54mm pitch 2x2-pin headers

Pin	Description	Pin	Description
1	Active	2	+3V
3	+3V	4	Link

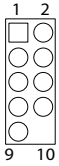


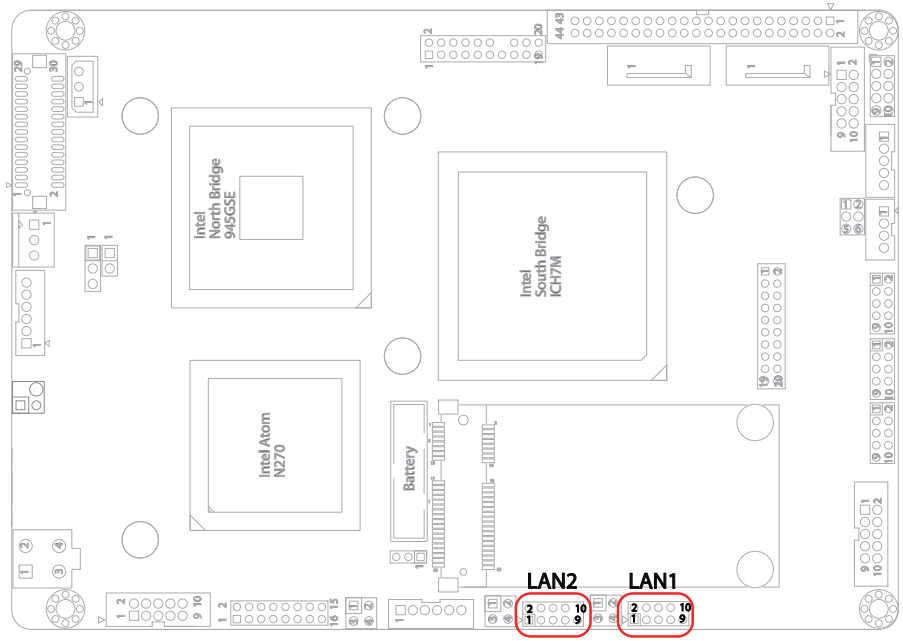


LAN1~2: Ethernet Connectors (16, 14)

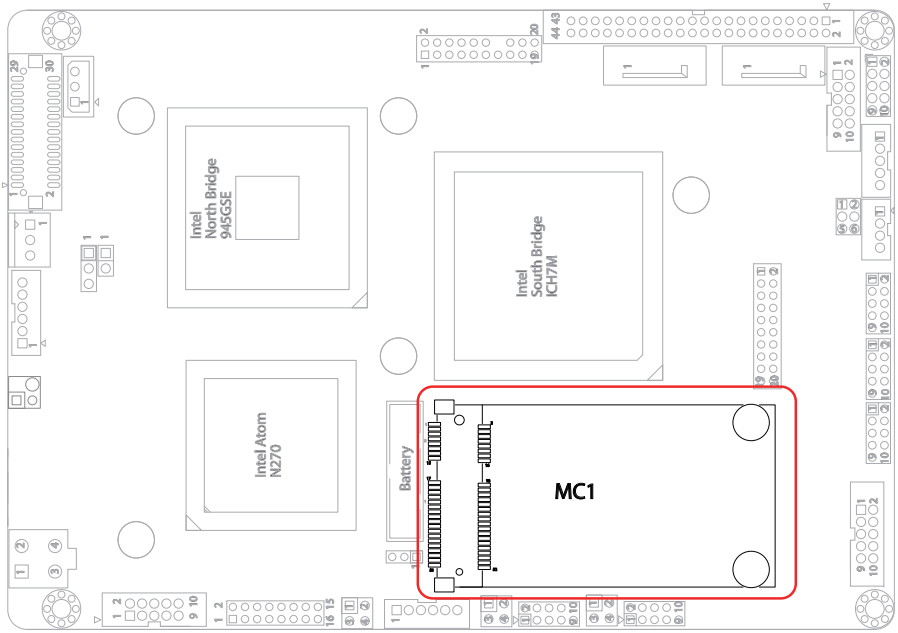
Connector type: 2.0mm pitch 2x5-pin headers

Pin	Description	Pin	Description
1	TX+/ MDI0+	2	TX/ MDI0-
3	RX+/ MDI1+	4	N/C/ MDI2+
5	N/C/ MDI2-	6	RX-/ MDI1-
7	N/C/ MDI3+	8	N/C/ MDI3-
9	N/C	10	N/C (Key)





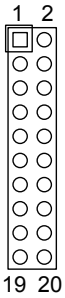
MC1: Mini-Card Slot (17)

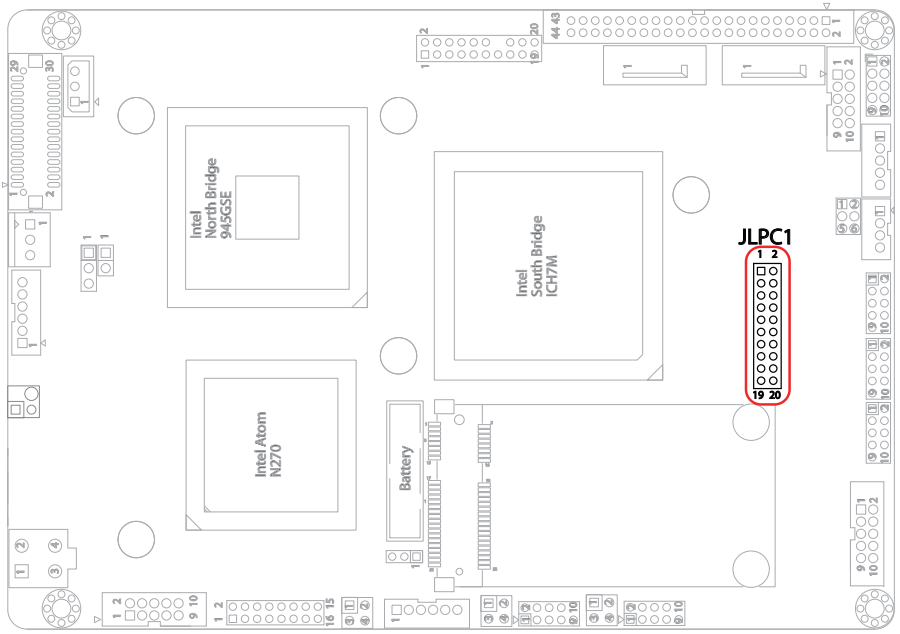


JLPC1: Low Pin Count Connector (18)

Connector type: 2.00mm pitch 2x10-pin headers

Pin	Description	Pin	Description
1	CLK	2	GND
3	LFRAME	4	N/C
5	LRESET	6	N/C
7	LAD3	8	LAD2
9	+3.3V	10	LAD1
11	LAD0	12	GND
13	N/C	14	N/C
15	+3.3V_SB	16	SERIRQ
17	GND	18	CLKRUN
19	PD	20	N/C





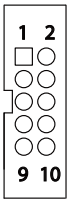
AUDIO1: AUDIO Connector (19)

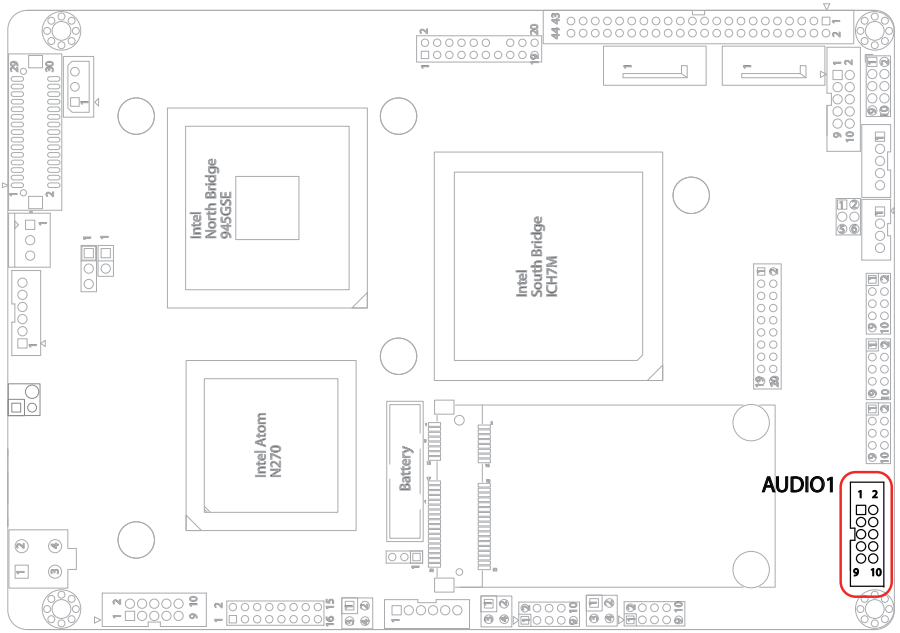
Connect a tape player or another audio source to the light blue Line-in connector to record audio on your computer or to play audio through your computer's sound chip and speakers.

Connect a micro-phone to the pink microphone connector to record audio to your computer.

Connector type: 2.00mm pitch 2x5-pin box headers.

Pin	Description	Pin	Description
1	Line-in Left	2	Line-in Right
3	GND	4	GND
5	MIC1	6	MIC2
7	GND	8	GND
9	Line-out Left	10	Line-out Right



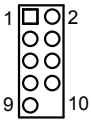


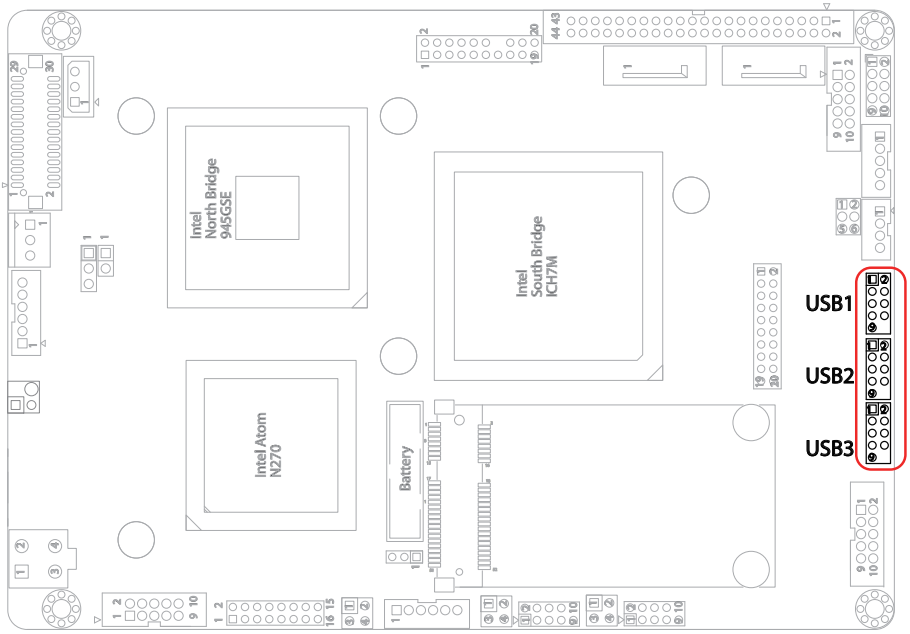
USB1~3: USB Connectors (22, 21, 20)

Connector type: 2.00mm pitch 2x5-pin headers.

USB1~3 support six USB 2.0 w/ 480Mb/s by pin headers

Pin	Description	Pin	Description
1	+5V	2	+5V
3	USBD-	4	USBD-
5	USBD+	6	USBD+
7	GND	8	GND
9	GND	10	N/C (Key)

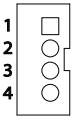


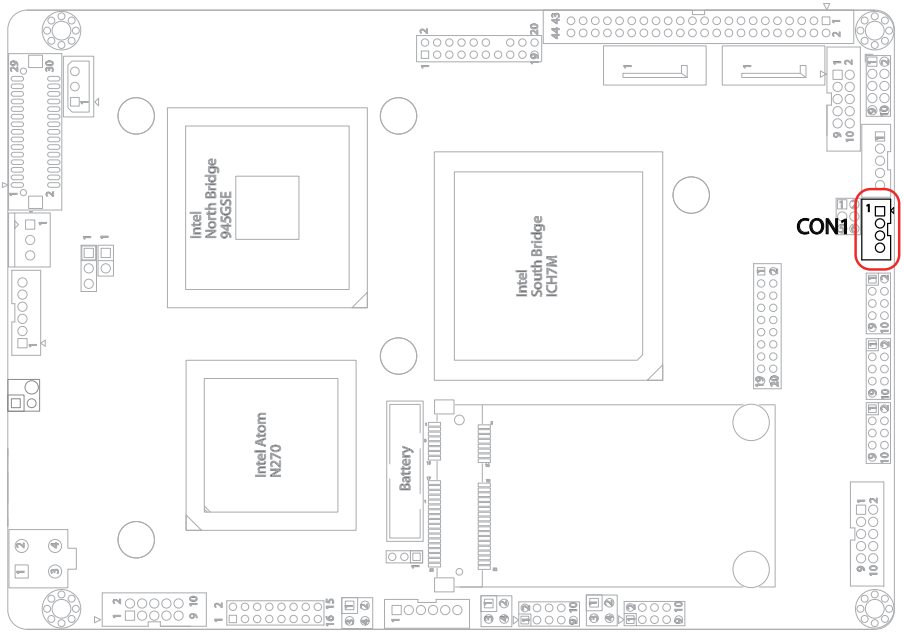


CON1: RS-422/ 485 Connector (24)

Connector type: 2.00mm pitch 1x4-pin box wafer connector

Pin	RS-422	RS-485
1	TX+	DATA+
2	TX-	DATA-
3	RX+	N/C
4	RX-	N/C

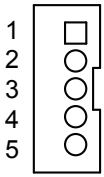


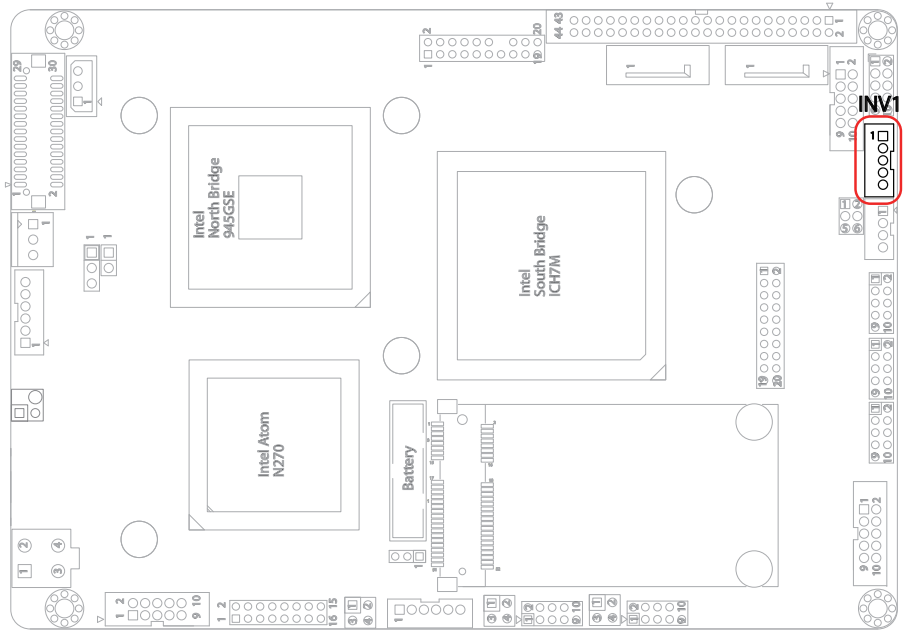


INV1: LCD Inverter Connector (25)

Connector type: 2.00mm pitch 1x5-pin box wafer connector.

Pin	Description
1	+12V
2	GND
3	Backlight on/off
4	Brightness control
5	GND



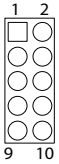


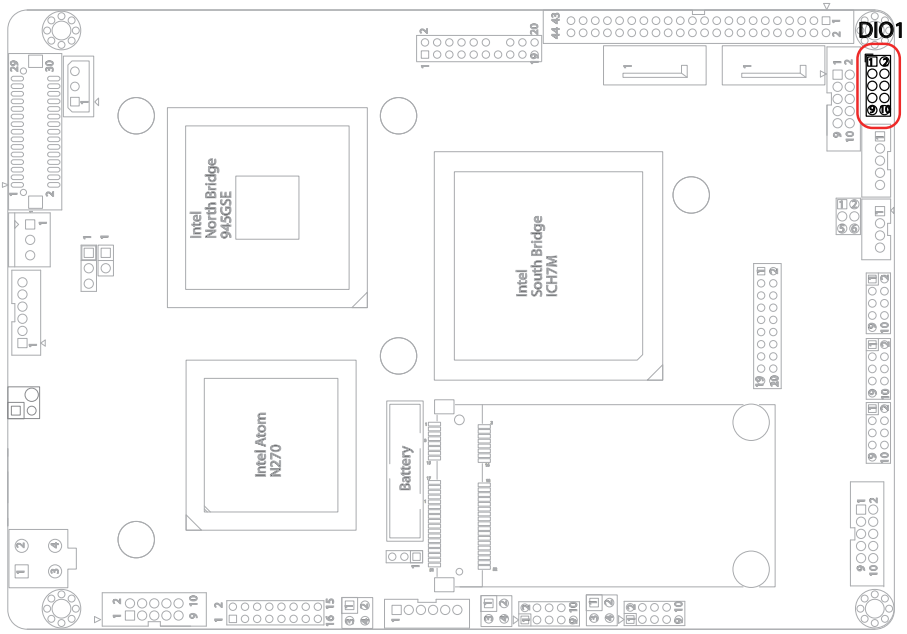
DIO1: Digital I/O Connector (26)

DIO1 is a 8-bit DIO connector w/ onboard 10-pin headers, supports programmable Input / Output.

Connector type: 2.00mm pitch 2x5-pin headers

Pin	Description	Pin	Description
1	DIO0	2	DIO1
3	DIO2	4	DIO3
5	DIO4	6	DIO5
7	DIO6	8	DIO7
9	+5V	10	GND





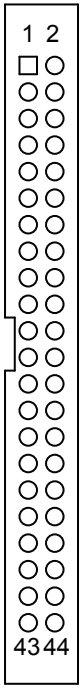
IDE1: IDE Connector (28)

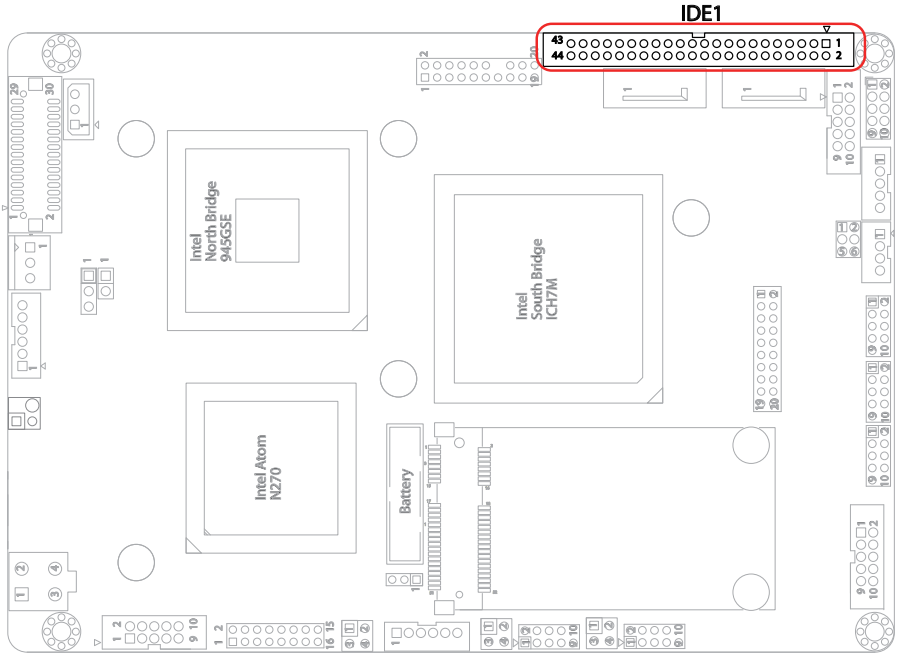
An IDE drive ribbon cable has two connectors to support two IDE devices. If a ribbon cable connects to two IDE drives at the same time, one of them has to be configured as Master and the other has to be configured as Slave by setting the drive select jumpers on the drive.

Consult the documentation that came with your IDE drive for details on jumper locations and settings. You must orient the cable connector so that the pin 1 (color) edge of the cable corresponds to pin 1 of the IDE connector.

Connector type: 2.00mm pitch 2x22-pin headers

Pin	Description	Pin	Description
1	IDE RESET	2	GND
3	DATA7	4	DATA8
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11
11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	N/C
21	REQ	22	GND
23	IO WRITE	24	GND
25	IO READ	26	GND
27	IO READY	28	IDSEL
29	DACK	30	GND
31	IRQ14	32	N/C
33	ADAD1	34	ATA66 DETECT
35	ADAD0	36	ADAD2
37	CS#1	38	CS#3
39	IDEACTP	40	GND
41	+5V	42	+5V
43	GND	44	N/C

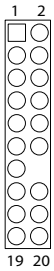



IDE1
43
44
1
2
Intel
North Bridge
945GSE
Intel
South Bridge
ICH7M
Intel Atom
N270
Battery

LPT1: Parallel Port or FDD Connector (29)

Connector type: 2.00mm pitch 2x10-pin headers.

Pin	Description	Pin	Description
1	STROBE#	2	AFD#
3	PTD0	4	Error#
5	PTD1	6	INIT#
7	PTD2	8	SLIN#
9	PTD3	10	GND
11	PTD4	12	GND
13	PTD5	14	N/C (Key)
15	PTD6	16	Busy
17	PTD7	18	PE
19	ACK#	20	Select



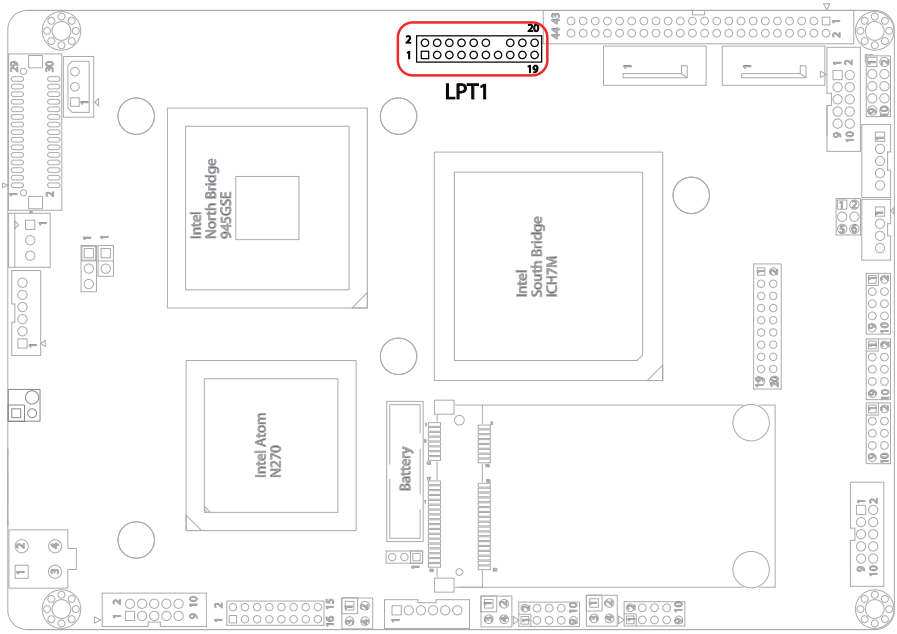
LPT1 can be configured as a connector floppy disk drive (FDD) interface through BIOS setup.

Pin	Description	Pin	Description
1	N/C	2	RWC#
3	RINDEX#	4	HEAD#
5	TRACK0#	6	DIR#
7	WP#	8	STEP#
9	RDATA#	10	GND
11	DSKCHG#	12	GND
13	N/C	14	N/C (Key)
15	N/C	16	MOB#
17	N/C	18	WD#
19	DSB#	20	WE#

BIOS Setup

The default is to set LPT1 as printer connector. To change the value, get into BIOS setup --> Integrated Peripheral --> Super IO Device.

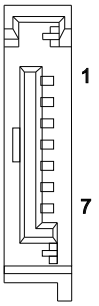
BIOS Option	Setting	Description
External FDD Controller	Enabled	Set as FDD connector
Onboard Parallel Port	Disabled	
External FDD Controller	Disabled	
Onboard Parallel Port	378/IRQ7	Set as Parallel Port

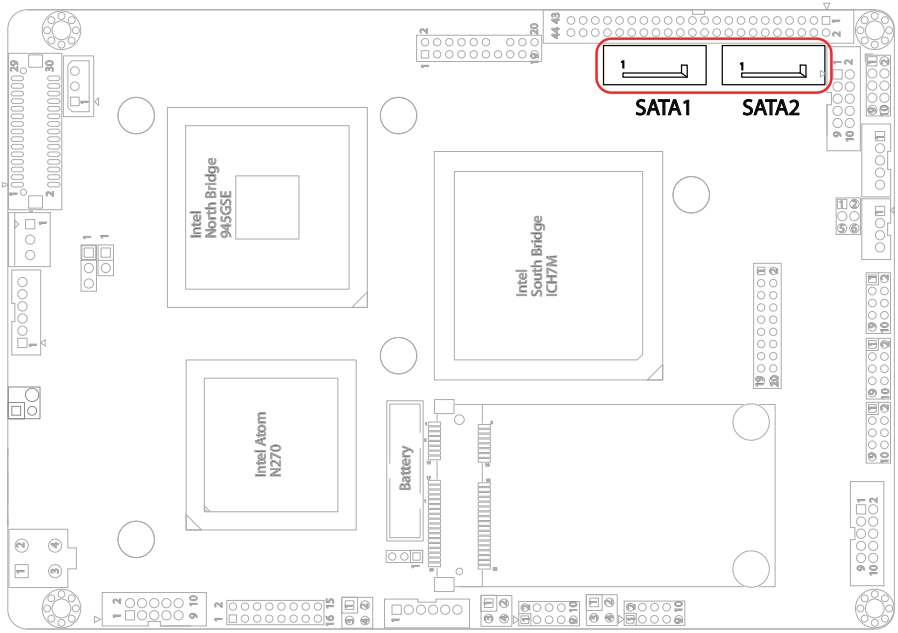

LPT1
20
19
2
1
Intel
North Bridge
945GSE
Intel
South Bridge
ICH7M
Intel Atom
N270
Battery

SATA1~ 2: Serial ATA Connectors (30, 31)

The CPU board on board supports two SATA connectors, second generation SATA drives transfer data at speeds as high as 150MB/s, twice the transfer speed of first generation SATA drives.

Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

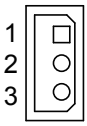


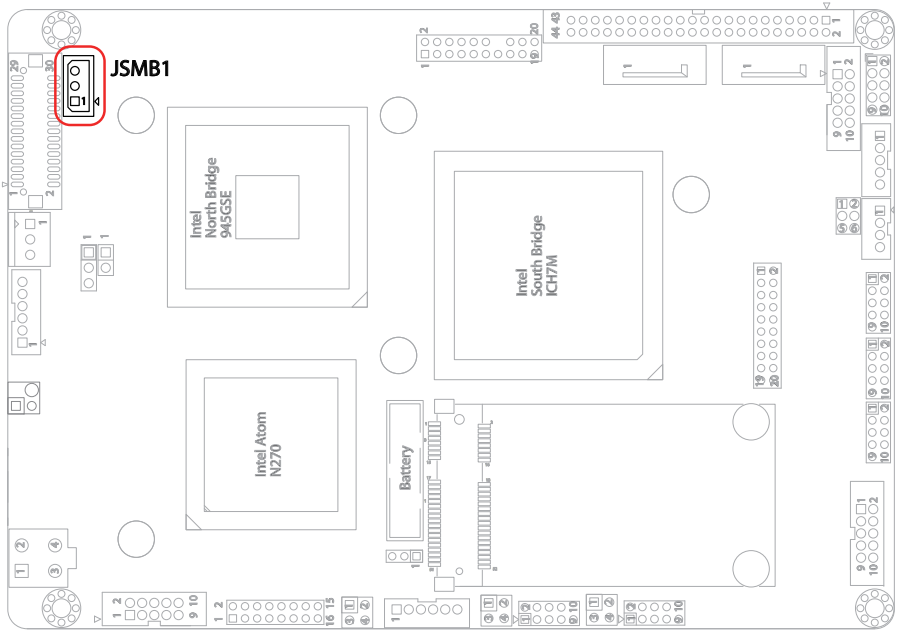


JSMB1: External SMBUS Connector (32)

Connector type: 2.54mm pitch 1x3-pin box wafer connector.

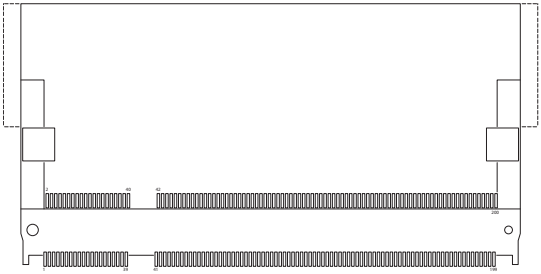
Pin	Description
1	Data
2	Clock
3	SMB_Alert#

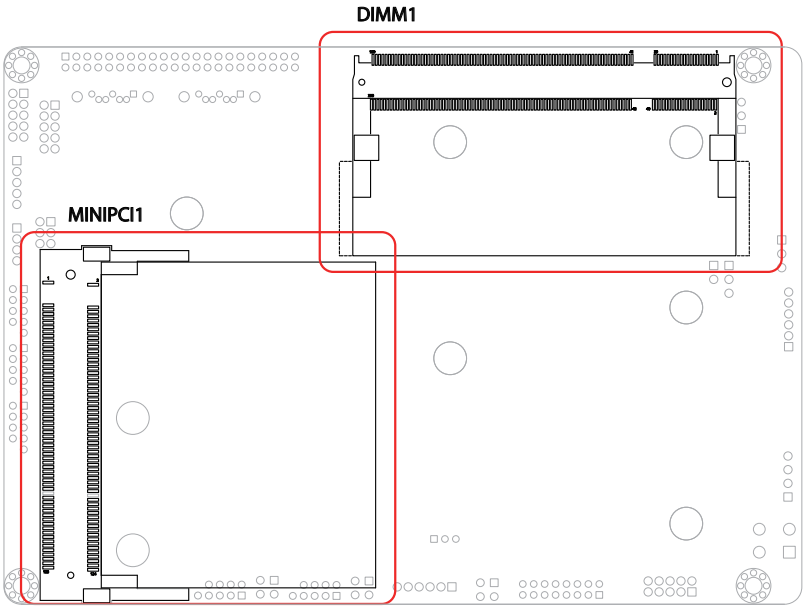




MINIPCI1: Mini PCI Socket (bottom side)

DIMM1: SO-DIMM Socket (bottom side)





2.3 The Installation Paths of CD Driver

Windows 2000 & XP

Driver	Path
CHIPSET	\CHIPSET\INF 9.2.0.1021\
LAN	\ETHERNET\REALTEK\8111_WINXP_5764
VGA	\GRAPHICS\INTEL_2K_XP_32\1432
AUDIO	\AUDIO\REALTEK_AC97\Win2K_XP_A406

Windows 7

Driver	Path
CHIPSET	\CHIPSET\INF 9.2.0.1021\
LAN	Windows 7 built-in LAN driver
VGA	\GRAPHICS\INTEL_WIN7_32\1930
AUDIO	\AUDIO\REALTEK_AC97\Win7_32_64_6305

Chapter 3

BIOS

3.1 BIOS Introduction

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility and configurations.

When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILILTY, press “Delete” once the power is turned on.

When the computer is shut down, the battery on the motherboard supplies the power for BIOS RAM.

The Main Setup screen lists the following information

System Overview

BIOS Version: displays the current version information of the BIOS

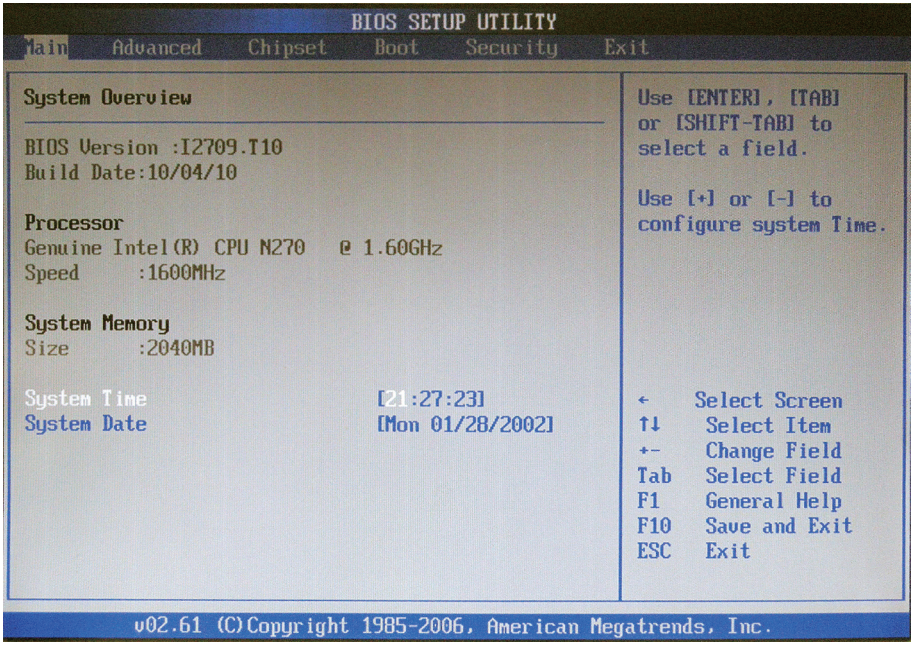
Build Date: the date that the BIOS version was made/updated

Processor (auto-detected if installed)

Speed: displays the processor speed

System Memory (auto-detected if installed)

Size: lists the memory size information



Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

"←""→"	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
"↓" "↑"	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select "OK" or "Cancel" for exiting and discarding changes. Use "←" and "→" to select and press "Enter" to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down -	Decrease the numeric value on a selected setup item / make change
F1	Activate "General Help" screen
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select "OK" or "Cancel" for exiting and saving changes. Use "←" and "→" to select and press "Enter" to confirm)

System Time

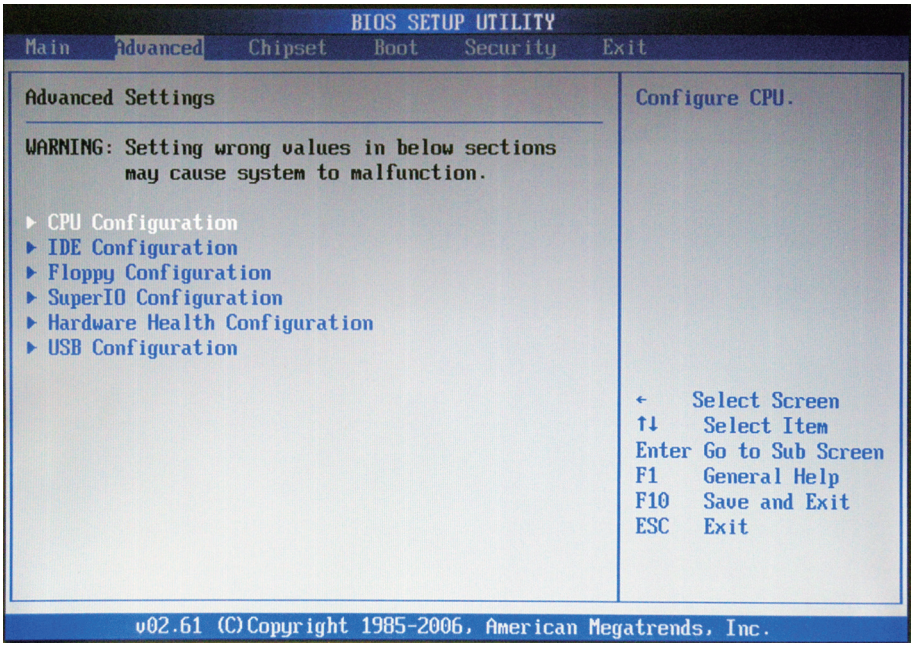
Set the system time.
The time format is:
Hour : 00 to 23
Minute : 00 to 59
Second : 00 to 59

System Date

Set the system date. Note that the 'Day' automatically changes when you set the date.
The date format is:
Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1999 to 2099

3.2 Advanced Settings

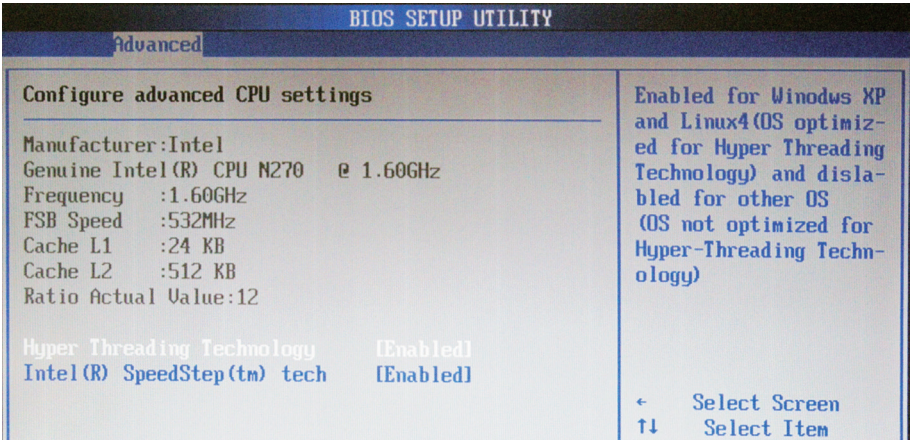
The “Advanced” screen provides the setting options to configure CPU, IDE, Super IO and other peripherals. You can use “←” and “→” keys to select “Advanced” and use the “↓” and “↑” to select a setup item.



Note: please pay attention to the “WARNING” part at the left frame before you decide to configure any setting of an item.

3.2.1 CPU Configuration

Press “Enter” on “CPU Configuration” and you will be able to configure the CPU on the “Configure advanced CPU settings” screen.



CPU Details

Manufacturer: shows the name of the CPU manufacturer
Frequency: indicates the processor speed
FSB Speed: the data flow speed of FSB (Front Side Bus)
Cache L1: shows the Cache L1 size for the CPU
Cache L2: shows the Cache L2 size for the CPU
Ratio Actual Value: actual value of clock ratio for the CPU

Hyper-Threading Technology

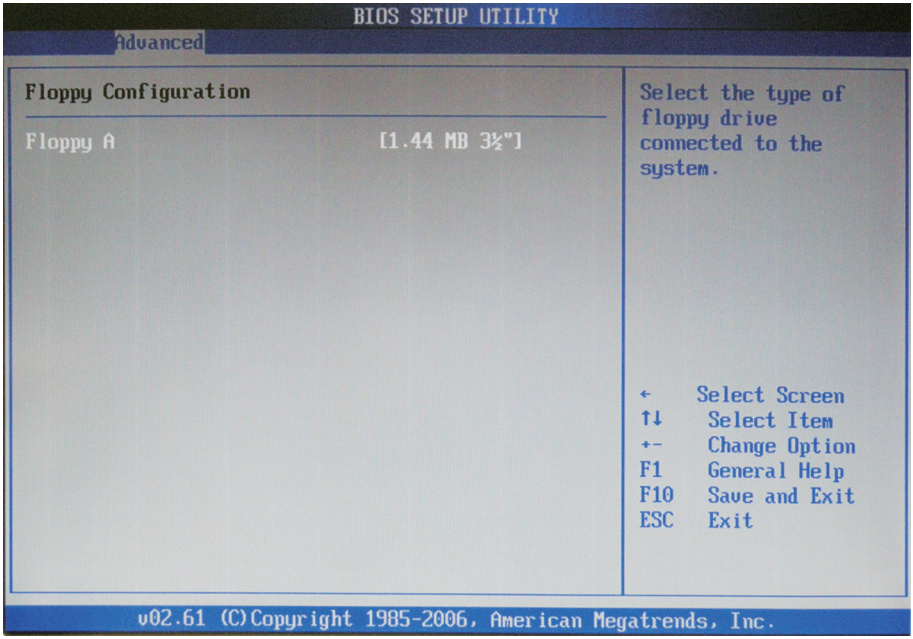
Enabled: activates the Hyper-Threading Technology for higher CPU threading speed. (Recommended)
Disabled: Disactivates the Hyper-Threading Technology.

Intel® SpeedStep™ Tech

Maximum: CPU speed is set to maximum.
Minimum: CPU speed is set to minimum.
Automatic: CPU speed controlled by Operating system.
Disabled: Default CPU speed.

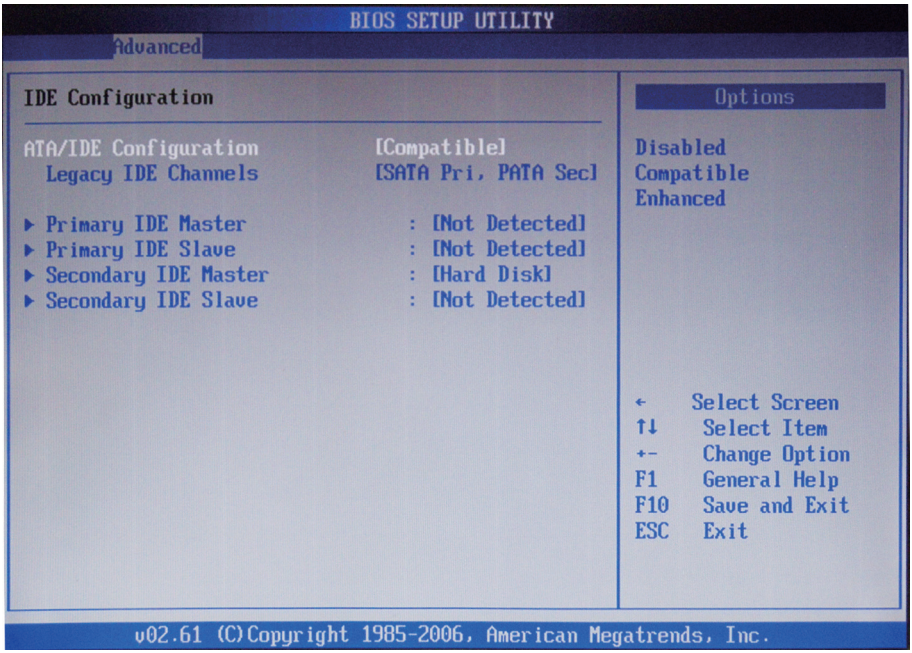
3.2.2 Floppy Configuration

Select the type of floppy drive connected to the system.



3.2.3 IDE Configuration

Select the “IDE Configuration to configure the IDE settings. When an item is selected, there is a status description appearing at the right. You can use “Page Up/+” and “Page Down/-” keys to change the value of a selected item.



ATA/IDE Configuration

Configures the options of ATA/IDE controllers connected to the board
Disabled: disables the ATA/IDE controllers connected to the board
Compatible: sets the ATA/IDE controllers to be compatible
Enhanced: sets the ATA/IDE controllers to be in enhanced mode

Legacy IDE Channels (SATA Pri, PATA Sec)

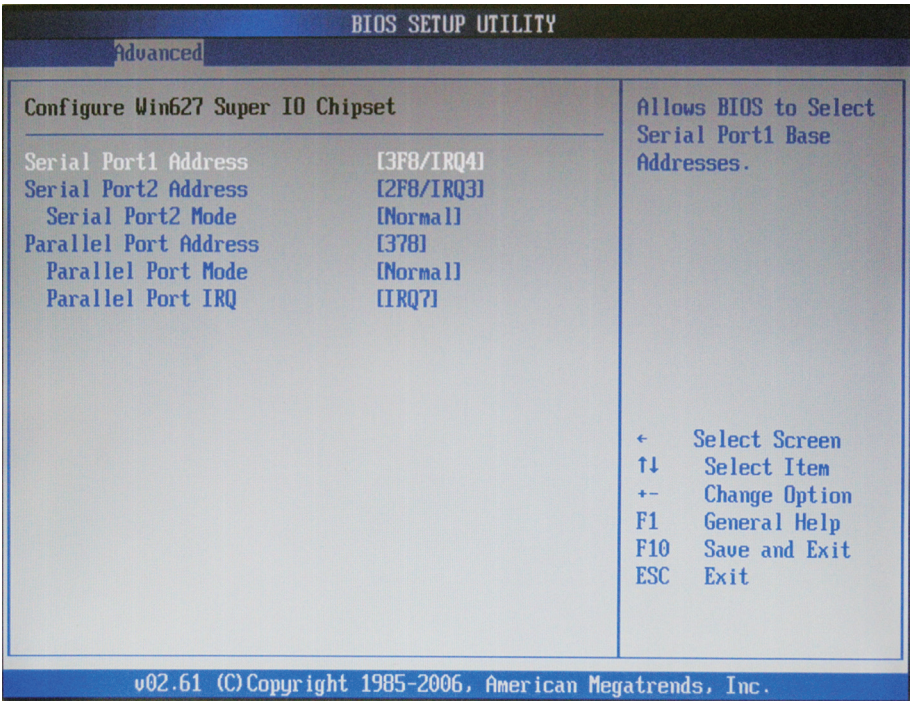
Specifies SATA or PATA controllers to be primary or secondary.

Primary IDE Master/Slave, Secondary IDE Master/Slave

The BIOS Setup displays all the available, connected IDE devices as well as the IDE status. You may enter a specific IDE device to do particular configurations. Press “Enter” to access the submenu of an IDE device on the list.

3.2.4 Super IO Configuration

Use “Super IO Configuration to specify address and modes for Serial Port and Parallel Port.



Serial Port1 / Port2 Address

Select an address and corresponding interrupt for the first and second serial ports.

The choice:

3F8/IRQ4
2E8/IRQ3
3E8/IRQ4
2F8/IRQ3
Disabled
Auto

Serial Port2 Mode

Allows BIOS to select mode for serial Port2.

Parallel Port Address

Select an address for the parallel port.
The choice:

- 3BC
- 378
- 278
- Disabled

Parallel Port Mode

Select an operating mode for the onboard parallel port. Select Normal, Compatible or SPP unless you are certain your hardware and software both support one of the other available modes.
The choice:

- SPP
- EPP
- ECP
- ECP + EPP
- Normal

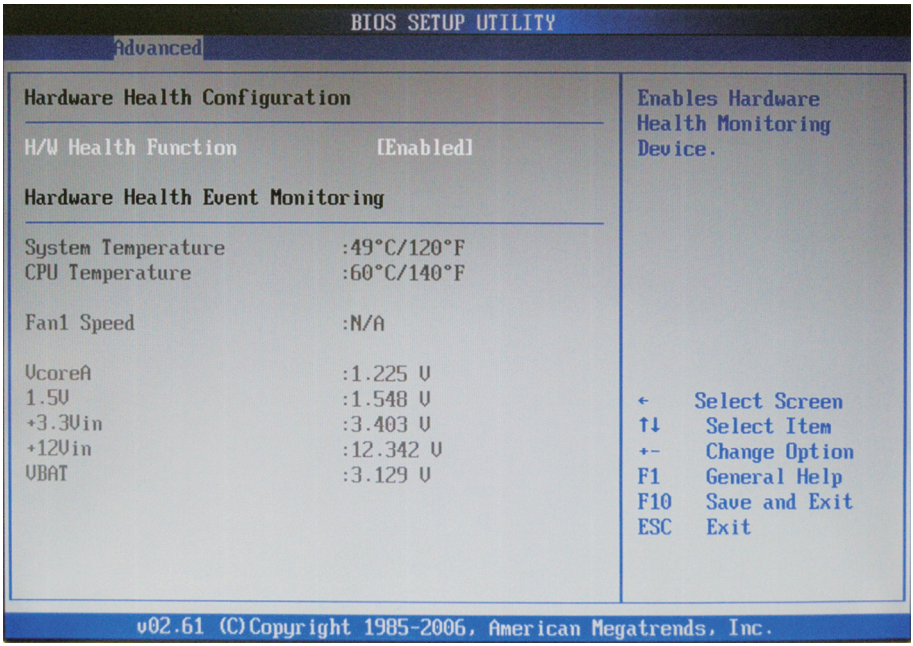
Parallel Port IRQ

Select an interrupt for the parallel port.
The choice:

- IRQ5
- IRQ7

3.2.5 Hardware Health Configuration

The “Hardware Health Configuration” lists out the temperature and voltage information that is being monitored. The default for “H/W Health Function” is “Enabled.



System/ CPU Temperature

Show you the current System / CPU fan temperature.

CPU / System / Chassis Fan Speed

Show you the current CPU / System / Chassis Fan operating speed.

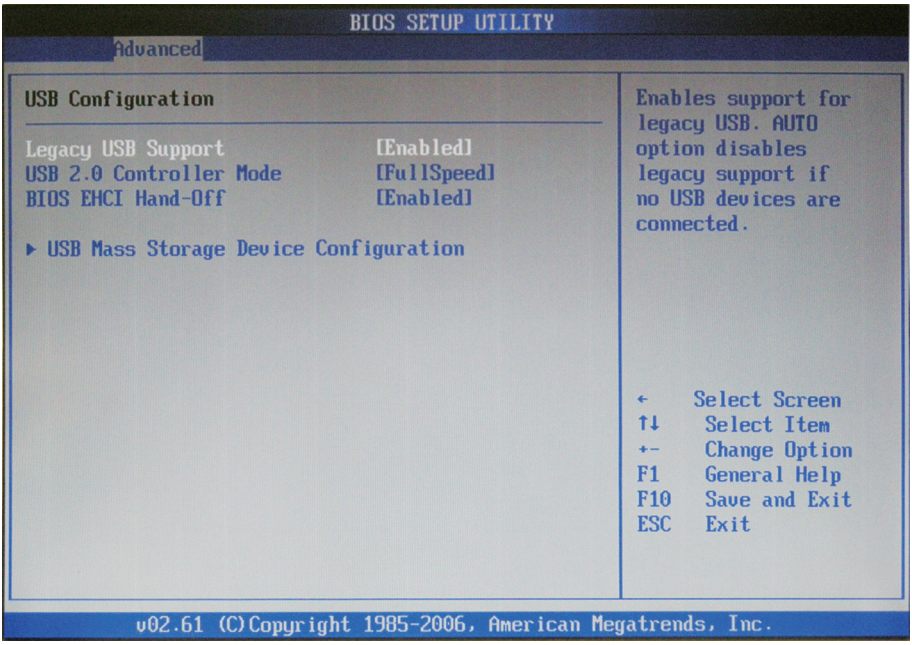
Vcore

Show you the voltage level of CPU (Vcore).

+1.5V / +3.3Vin / +12Vin / VBAT

Show you the voltage level of the +1.5V, +3.3Vin, +12Vin, and battery.

3.2.6 USB Configuration



Legacy USB Support

Enables support for legacy USB. AUTO option disables legacy support if no USB devices are connected.

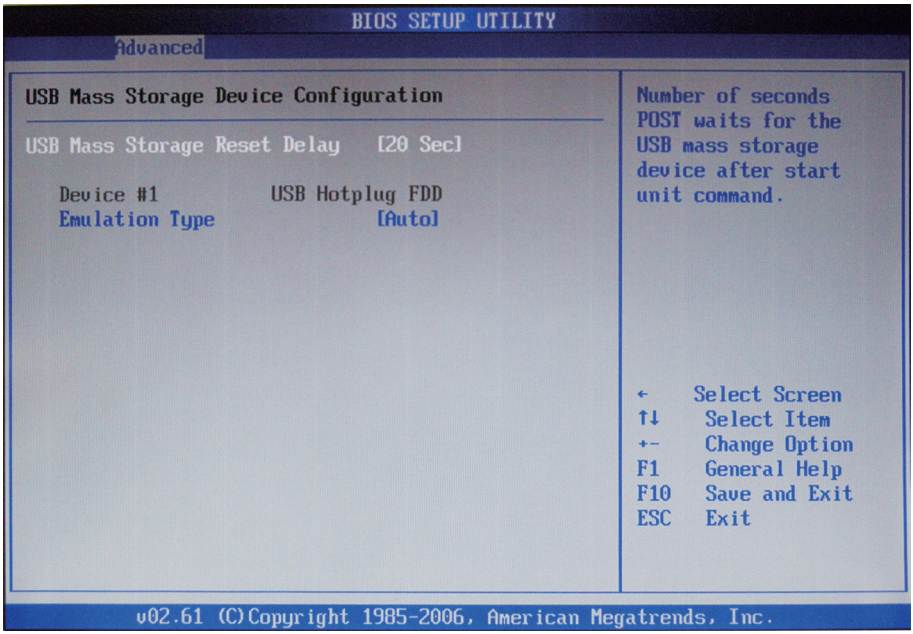
USB 2.0 Controller Mode

Configures the USB 2.0 controller in High Speed (480Mbps) or Full Speed (12Mbps).

BIOS EHCI Hand-Off

Enabled: enables the EHCI Hand-Off function by BIOS
Disabled: disables the EHCI Hand-Off function by BIOS
Note: this setting potion allows you to enable EHCI Hand Off if your computer operating system does not support it.
EHCI is the abbreviation for Enhanced Host Controller Interface which is necessary for high speed USB operation.

USB Mass Storage Device Configuration



USB Mass Storage Reset Delay

Number of seconds POST waits for the USB mass storage device after start unit command.

Emulation Type

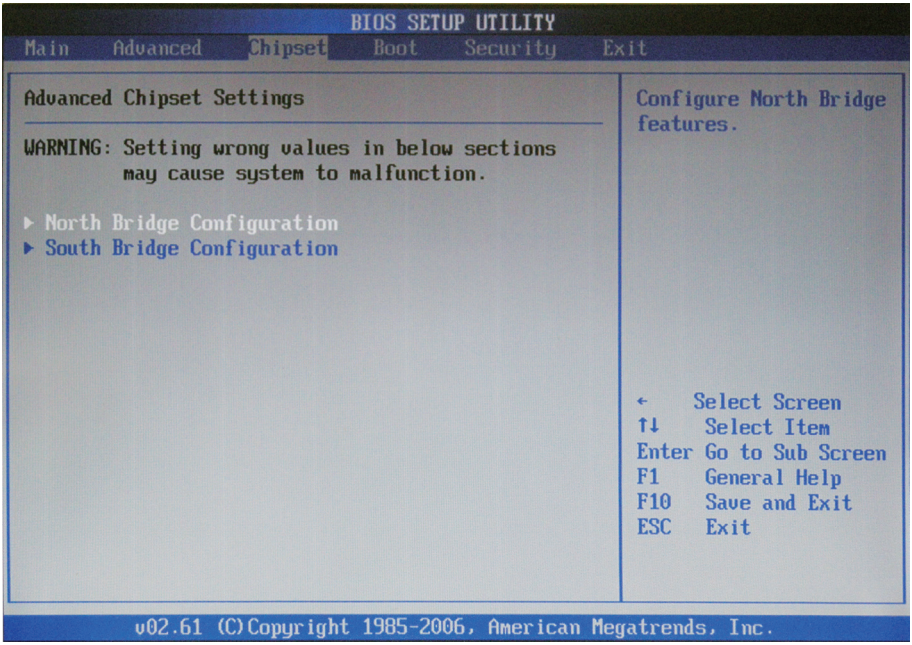
If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to BOOT as FDD. (Ex. ZIP drive).

Note

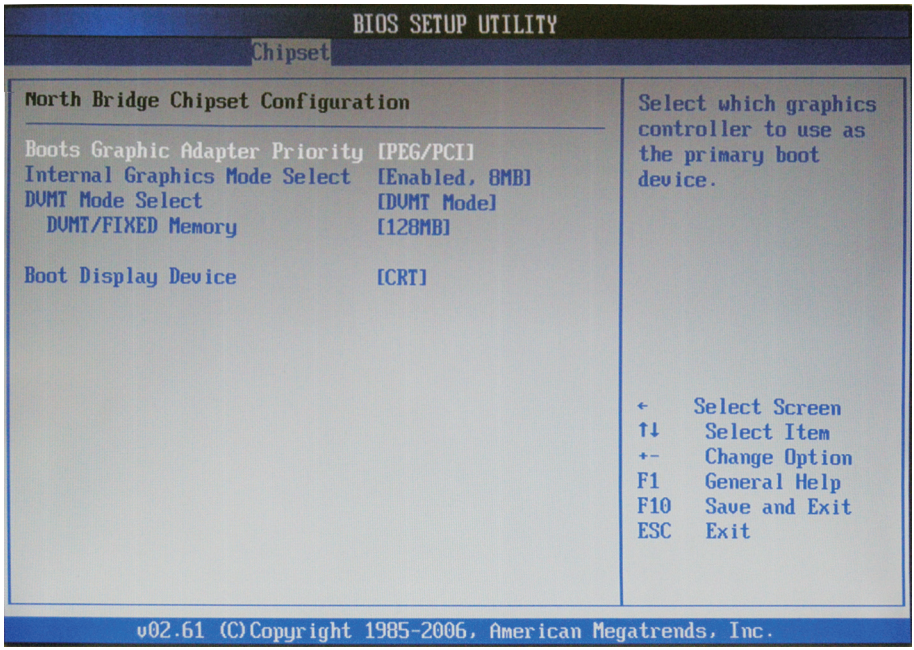
If “Auto” is selected, USB device with storage less than 530MB will be emulated as Floppy and remain as hard drive. Forced FDD option can be used to force a HDD formatted drive to “BOOT” as FDD (for example, ZIP drive)

3.3 Advanced Chipset Settings

Select “Chipset” to access to “North Bridge Configuration” and “South Bridge Configuration”. You can enter the sub menu of the two configuration options.



3.3.1 North Bridge Chipset Configuration



Boots Graphic Adapter Priority

Select which graphics controller to use as the primary boot device.
The Choice: IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI

Internal Graphic Mode Select

Select the amount of system memory used by the Internal graphics device.
The Choice: Disabled; Enabled, 1MB; Enabled, 8MB

DVMT Mode

The Choice: FIXED mode, DVMT (Default), Combo Mode.

DVMT/FIXED Memory Size

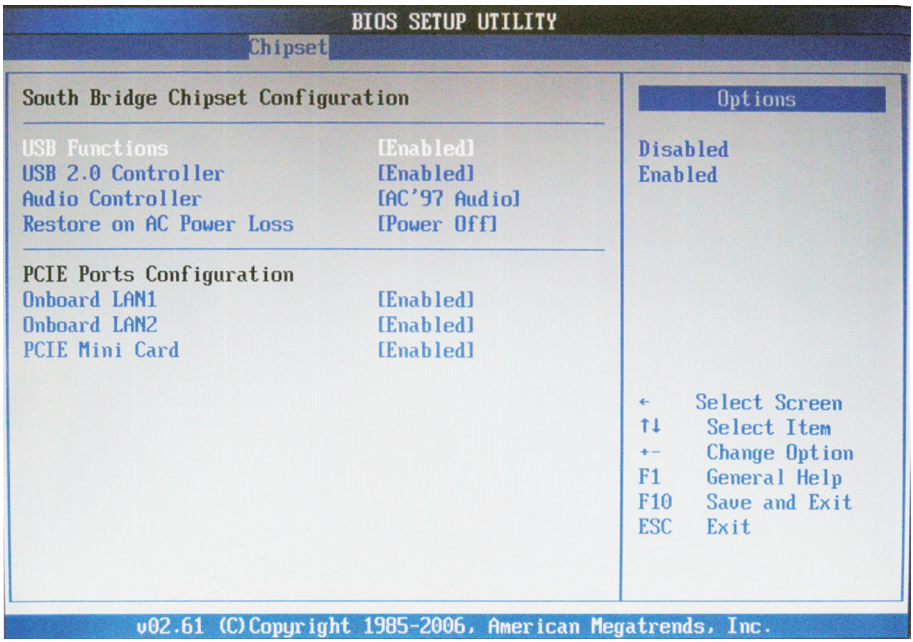
Setting: 64MB, 128MB (Default), Maximum DVMT.

Boot Display Device

Boot setting for the display device connected to the computer, such as “External CRT” monitor.
The Choice: CRT, SDVO LVDS, TV, CRT + SDVO LVDS

3.3.2 South Bridge Chipset Configuration

Normally, the south bridge controls the basic I/O functions, such as USB and audio. This screen allows you to access to the configurations of the I/Os.



USB Funtion

This item allows you to active USB ports.

The Choice: Disabled, Enabled

USB 2.0 Controller

Select “Enabled” if your system contains a Universal Serial Bus 2.0 (USB 2.0) controller and you have USB peripherals.

The Choice: Enabled, Disabled.

AUDIO Controller

This item allows you to select the chipset family to support AC97 Audio Controller.

The Choice: AC’97 Audio, Disabled.

PCIE Ports Configuratin

Onboard LAN1 / LAN2

Select “Enabled” if your system has a LAN device installed on the system board and you wish to use it.

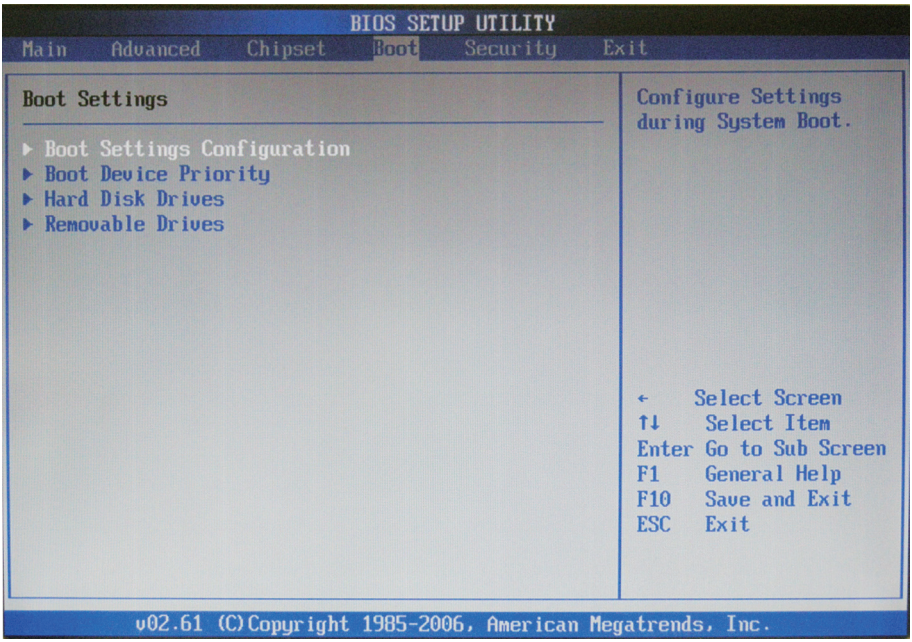
The Choice: Enabled, Disabled.

PCIE Mini Card

Select “Enabled” if your system has a Mini Card device installed on the system board and you wish to use it.

The Choice: Enabled, Disabled.

3.4 Boot Settings



Boot Setting Configuration

Press Enter the sub menu for boot setting.

Boot Device Priority

Access to the sub menu for boot device priority.

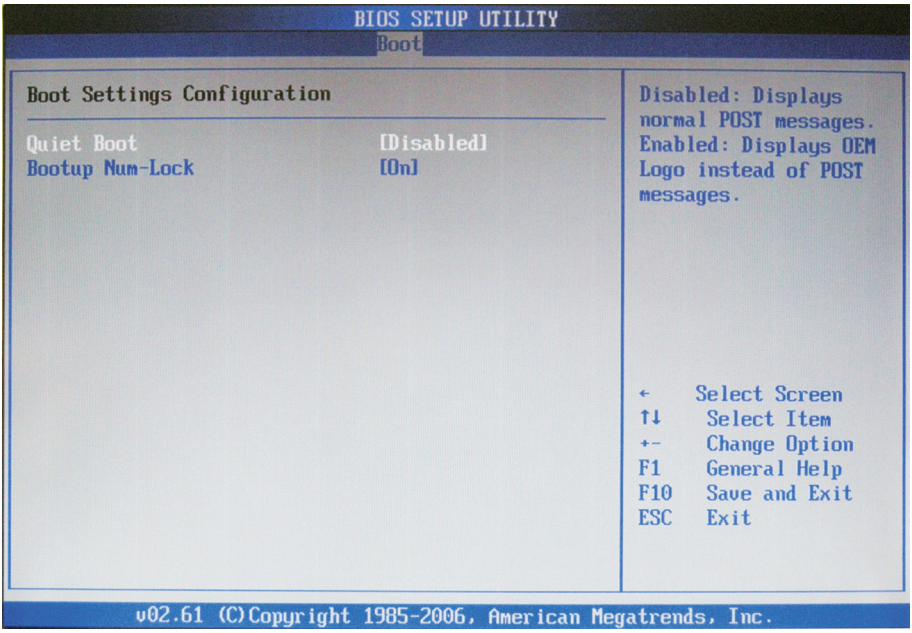
Hard Disk Drives

Configure the boot settings for the Hard Disk Drives connected to the system.

Removable Drives

Press Enter and it shows Bootable and Removable drives.

3.4.1 Boot Settings Configuration



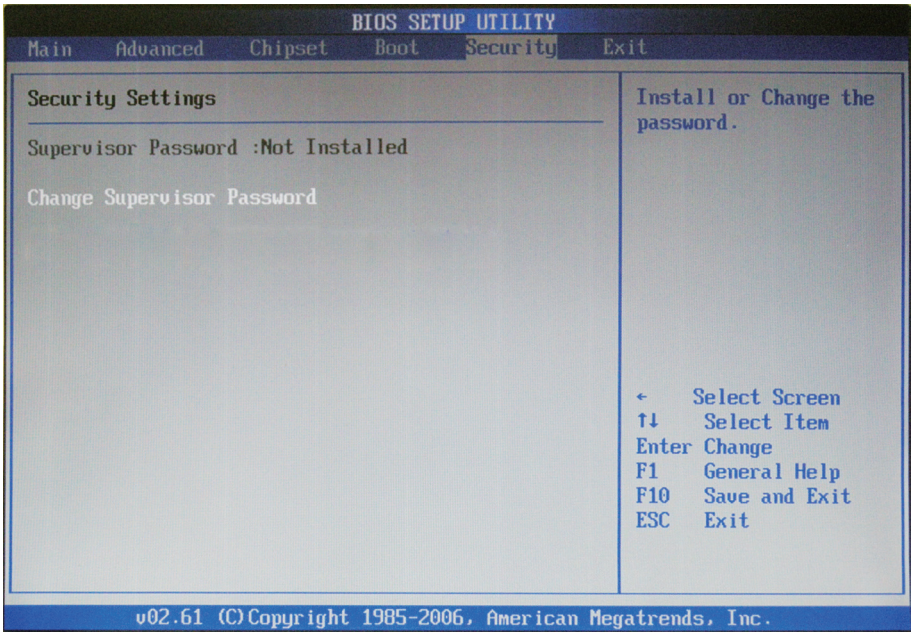
Quiet Boot

Displays normal POST messages when it's selected as "Disabled".
When it is set as "Enabled", OEM messages will be displayed instead of POST messages. The default is "Disabled".

Bootup Num-Lock

Modifies Number Lock setting when the system boots up. Select "On" to automatically enable the Number Lock on keyboard when the system is booting up.

3.5 Security



Supervisor Password & User Password

You can set either supervisor or user password, or both of them. The differences between are:

Set ***Supervisor Password***: Can enter and change the options of the setup menus.

Set ***User Password***: Just can only enter but do not have the right to change the options of the setup menus. When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD:

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <ESC> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

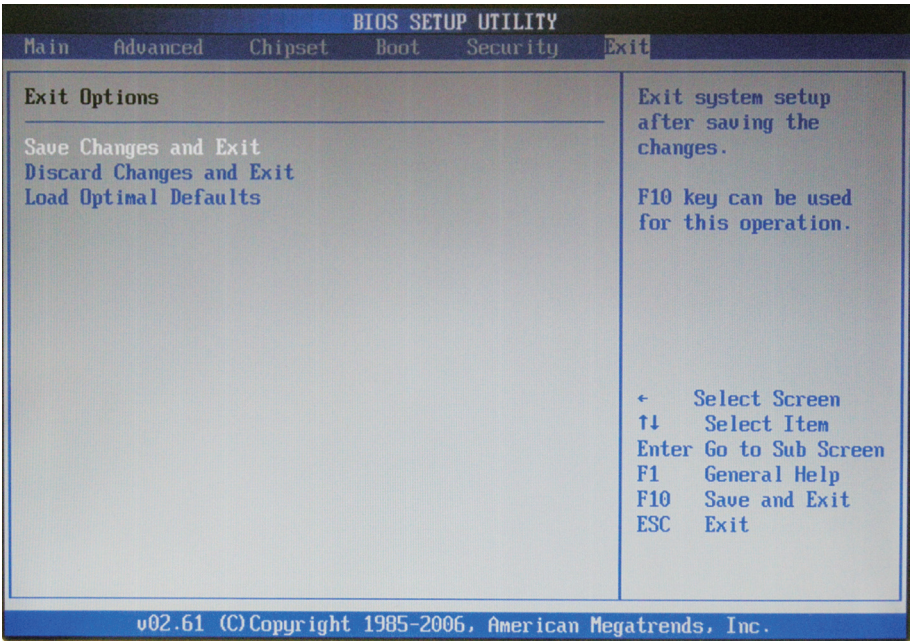
PASSWORD DISABLED.

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If set to “Setup”, prompting only occurs when trying to enter Setup.

3.6 Exit Options



Save Changes and Exit

Pressing <Enter> on this item asks for confirmation:

Save configuration changes and exit setup?

Pressing <OK> stores the selection made in the menus in CMOS - a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

Discard Changes and Exit

Exit system setup without saving any changes.
You can also press <ESC> to activate this function.

Load Optimal Defaults

When you press <Enter> on this option, a message dialog box will appear asking for your confirmation:

Load Optimal Defaults?
[OK] [Cancel]

Press [OK] to load the BIOS Optimal Default values for all the setup options.
You can also press <F9> key to enable this operation.

3.7 Beep Sound codes list

3.7.1 Boot Block Beep codes

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

3.7.2 POST BIOS Beep codes

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

3.7.3 Troubleshooting POST BIOS Beep codes

Number of Beeps	Description
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

3.8 AMI BIOS Checkpoints

3.8.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS *(Note)*:

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processo (BSP) initialization like microcode update, frequency and other CPU cirtical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is deisabled. Perfrom keyboard controller BAT test. Save power-on CPUID value in scretch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enabled CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Perfroms main BIOS checksum and updates recovery status accordingly.

D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows tocheckpoint E0. Seed *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether in memory.
D8	The Tuntime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POS (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
DC	System is saking from ACPI S3 state.
E1 - E8 EC - EE	OEM memory detection / configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to be next.

3.8.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS *(Note)*:

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L2 cache is enabled.
E9	Set up floppy controller and data. Attempt to red from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.

FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

3.8.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS *(Note)*:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system.
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor

C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information. USB controllers are initialized at this point.

39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to theuser and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disalbe NMI as selected.
90	Initialization of system management interrupt by invoking all handlers.
A1	Lian-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.

A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for userinput at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

3.8.4 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system buses. The following table describes the main checkpoints where the DIM module is accessed *(Note)*:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble “X” indicates the function number that is being executed. “X” can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.

3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = On-board System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

3.8.5 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events *(Note)*:

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

Note:
Please note that checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Chapter 4

Appendix

4.1 I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
00000000 - 0000000F	DMA Controller
00000080 - 0000009F	DMA Controller
000000C0 - 000000DF	DMA Controller
00000020 - 00000021	Programmable Interrupt Controller
000000A0 - 000000A1	Programmable Interrupt Controller
00000040 - 00000043	System Timer
00000044 - 00000047	System Timer
00000060 - 00000064	Keyboard Controller
00000070 - 00000073	System CMOS/Real Time Clock
000000F0 - 000000FF	Math Co-processor
000001F0 - 000001F7	Primary IDE
00000274 - 00000277	ISAPNP Read Data Port
00000279, 00000A79	ISAPNP Configuration
000002F8 - 000002FF	Communications Port (COM2, If use)
00000378 - 0000037A	Parallel Port (If use)
000003B0 - 000003BF	MDA/MGA
000003C0 - 000003CF	EGA/VGA
000003D4 - 000003D9	CGA Analog RGB register
000003F0 - 000003F7	Floppy Diskette
000003F6 - 000003F6	Primary IDE
000003F8 - 000003FF	Communications Port (COM1, If use)
00000400 - 0000041F	South Bridge SMB
000004D0 - 000004D1	IRQ Edge/Level Control Ports
00000500 - 0000053F	South Btidge GPIO
00000800 - 0000087F	ACPI
00000A00 - 00000A07	PME

00000A10 - 00000A17	Hardware Monitor
00000CF8	PCI Configuration Address
00000CFC	PCI Configuration Data

4.2 Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System Timer
IRQ 1	Keyboard Controller
IRQ 2	VGA and Link to Secondary PIC
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 5	PCI Device
IRQ 6	Standard Floppy Disk Controller
IRQ 7	Parallel Port
IRQ 8	System CMOS/real time clock
IRQ 9	Microsoft ACPI-Compliant System
IRQ 10	PCI Device
IRQ 11	PCI Device
IRQ 12	PS/2 Compatible Mouse
IRQ 13	FPU Exception
IRQ 14	IDE Controller
IRQ 15	PCI Device

4.3 BIOS memory mapping

Address	Device Description
00000h - 9FFFFh	DOS Kernel Area
A0000h, BFFFFh	EGA and VGA Video Buffer (128KB)
C00000h - CFFFFh	EGA/VGA ROM
D0000h - DFFFFh	Adaptor ROM
E00000h - FFFFFh	System BIOS

4.4 Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitoring the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. Then, WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming. Below are the source codes written in assembly & C, please take them for WDT application examples.

Assembly Code

```
;-- Initial W83627hf --
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 87h
        out     DX, AX          ;
        out     DX, AX          ; initial W83627HF start
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 2Bh
        out     DX, AL          ; Select CR2B
        mov     AL, 00h
        inc     DX
        out     DX, AL          ; Set CR2B bit 4=0, PIN89=WDTO
;--
        mov     AX, 2Eh
```

```
        mov     DX, AX
        mov     AL, 07h
        out     DX, AL          ; Point to Logical Device Selector
        mov     AL, 08h
        inc     DX
        out     DX, AL          ; Select Logical Device 8
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 30h
        out     DX, AL          ; select CR30
        mov     AL, 01h
        inc     DX
        out     DX, AL          ; update CR30 to 01h
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 0F0h
        out     DX, AL          ; select CRF0
        mov     AL, 00h
        inc     DX
        out     DX, AL          ; set CRF0=00h, output
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 0F5h
        out     DX, AL          ; select CRF5, WDT Timer unit
        mov     AL, 00h         ; bit2 =0 ->second ; bit2 =1 -> minute
        inc     DX
        out     DX, AL          ; update CRF5 bit2 to 00h
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 0F6h
        out     DX, AL          ; select CRF6, WDT Timer
        mov     AL, 05h
        inc     DX
        out     DX, AL          ; update CRF6 to 5 unit
;---
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, AAh
        out     DX, AX
;-- end
```

C Language Code

```
/*-----     Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

/*-----     routing, sub-routing -----*/

void main()

{
          outportb(0x2e, 0x87);       /* initial IO port twice */
          outportb(0x2e, 0x87);

          outportb(0x2e, 0x2B);       /* select CR2B */
          outportb(0x2e+1, 0x00);     /* update CR2B bit4 to 00h */
                                      /* Set PIN89 as WDTO */

          outportb(0x2e, 0x07);       /* point to logical device selector */
          outportb(0x2e+1, 0x08);     /* select logical device 8 */
          outportb(0x2e, 0x30);       /* select CR30 */
          outportb(0x2e+1, 0x01);     /* update CR30 to 01h */
          outportb(0x2e, 0xf0);       /* select CRF0 */
          outportb(0x2e+1, 0x00);     /* update CRF0 to 00h */
          outportb(0x2e, 0xf5);       /* select CRF5 to set timer unit */
          outportb(0x2e+1, 0x00);     /* update CRF5 bit2, 0:sec; 1:Min. */
          outportb(0x2e, 0xF6);       /* select CRF6 */
          outportb(0x2e+1, 0x05);     /* update CRF6 to 05h (5 sec) */

          outportb(0x2e, 0xAA);       /* stop program W83627HF, Exit */
}
```

4.5 Digital I/O Setting

Below are the source codes written in assembly & C, please take them for Digital I/O application examples.

Assembly Code

```
;-- Initial W83627hf --
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 87h
        out     DX, AX          ;
        out     DX, AX          ; initial W83627HF start
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 2Ah
        out     DX, AL          ; Select CR2A
        mov     AL, 0FCh
        INC     DX
        out     DX, AL          ; Set CR2A bit 7=1 as GPIO port 1
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 07h
        out     DX, AL          ; Point to Logical Device Selector
        mov     AL, 07h
        inc     DX
        out     DX, AL          ; Select Logical Device 7
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 30h
        out     DX, AL          ; select CR30
        mov     AL, 01h
        inc     DX
        out     DX, AL          ; set bit0=1, GPIO port 1 active
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 0F0h
        out     DX, AL          ; select CRF0, GP I/O select
        mov     AL, 00h
```

```
        inc     DX
        OUT     DX, AL          ; bit7~bit0 0:output  1:input
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 0F1h
        out     DX, AL          ; select CRF1, Data Register
        mov     AL, 0FFh
        inc     DX
        out     DX, AL          ; set all GPIO pin output 1
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 0F1h
        out     DX, AL          ; select CRF1, Data Register
        mov     AL, 000h
        inc     DX
        out     DX, AL          ; set all GPIO pin output 0
;---
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, AAh
        out     DX, AX
;-- end
```

C Language Code

```
/*-----     Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

/*-----     routing, sub-routing -----*/

void main()

{
        outportb(0x2e, 0x87);       /* initial IO port twice */
        outportb(0x2e, 0x87);

        outportb(0x2e, 0x2a);       /* Select CR2A */
        outportb(0x2e+1, 0xfc);     /* set CR2A bit7=1 as GPIO port 1*/

        outportb(0x2e, 0x07);       /* point to logical device */
        outportb(0x2e+1, 0x07);     /* select logical device 7 */

        outportb(0x2e, 0x30);       /* select CR30 */
        outportb(0x2e+1, 0x01);     /* set bit0=1, GPIO port 1 active */

        outportb(0x2e, 0xf0);       /* select CRF0, GP I/O select */
        outportb(0x2e+1, 0x00);     /* bit7~bit0 0:output  1:input */

        outportb(0x2e, 0xf1);       /* select CRF1, Data Register */
        outportb(0x2e+1, 0xff);     /* set all GPIO pin output 1 */

        outportb(0x2e, 0xf1);       /* select CRF1, Data Register */
        outportb(0x2e+1, 0x00);     /* set all GPIO pin output 0 */

        outportb(0x2e, 0xAA);       /* stop program W83627HF, Exit */

}
```

This page is intentionally left blank.