EmCORE-i2501

3.5” Compact Board

User’s Manual

Version 1.1

2013.05

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Chapter 1

Introduction

1.1 Copyright Notice

All Rights Reserved.

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

1.2 Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

> Warning
>
> This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

1.3 About This User's Manual

This user's manual provides general information and installation instructions about the product. This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. please consult your vendor before further handling.

1.4 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

1.5 Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

1.6 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw

E-mail:info@arbor.com.tw

1.7 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.8 Packing List

Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

1 x EmCORE-i2501 3.5" Compact Board with heatsink
1 x Power cable

1 x Driver CD

1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

1.9 Ordering Information

EmCORE-i2501-N26	Intel® Atom™ N2600 3.5" Compact Board with CFast socket
EmCORE-i2501D-N26 (BTO)	Intel® Atom™ N2600 3.5" Compact Board with 8GB NANDrive
EmCORE-i2501-D25	Intel® Atom™ D2550 3.5" Compact Board with CFast socket
EmCORE-i2501D-D25 (BTO)	Intel® Atom™ D2550 3.5" Compact Board with 8GB NANDrive

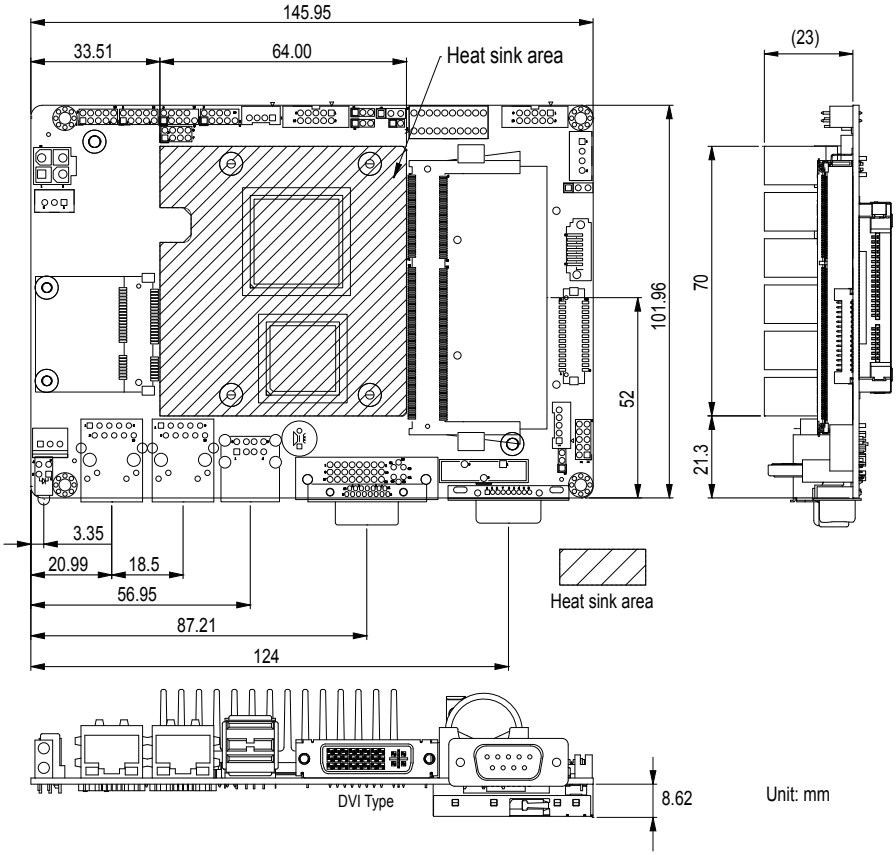
Optional Accessories

CBK-06-2501-00	Cable Kit • 1 x COM port cable • 1 x audio cable • 2 x USB cables • 1 x SATA cable • 1 x SATA power cable

1.10 Specifications

Form Factor	3.5" Compact Board
CPU	Soldered onboard Intel® Atom™ N2600 at 1.6GHz or D2550 at 1.86GHz processor
Chipset	Intel® PCH NM10
System Memory	1 x 204-pin DDR3 SO-DIMM socket, supporting 1066MHz SDRAM up to 4GB (D2550)/ 2GB (N2600)
Graphics Chipset	Integrated Intel® Graphics Media Accelerator 3650/ 3600
Graphics Interface	Analog RGB supports resolution up to 1920x1200@60Hz
	DVI-I: support Analog RBG up to 1920 x 1200 @60Hz or DVI up to 1920 x 1200 @60Hz
	Single Channel: - 18-bit LVDS for EmCORE-i2501-N26 - 24-bit LVDS for EmCORE-i2501-D25
	Support dual independent display
Ethernet	2 x Intel® 82583V PCIe Gigabit Ethernet Controllers
I/O Chips	Fintek F81866D
BIOS	AMI UEFI BIOS
Audio	Realtek ALC662 5.1 Channel HD Audio CODEC, Mic-in/ Line-in/ Line-out
Storage	1 x Serial ATA port with 300MB/s HDD transfer rate
	1 x CFast socket or soldered onboard 8GB NANDriver (Alternative)
Serial Port	2 x COM ports (1 x RS-232 port, 1 x RS-232/422/485 port selectable)
Universal Serial Bus	6 x USB 2.0 ports
Digital IO	8-bit programmable Digital Input/ Output
Expansion Bus	1 x Mini-card socket (half size)
Power Requirement	+12V DC
Operation Temp.	-20˚C ~ 70˚C (-4˚F ~ 158˚F)
Operating Humidity	10 ~ 95% @ 70ºC (non-condensing)
Watchdog Timer	1~255 levels reset
Dimension (L x W)	146 x 102 mm (5.7” x 4.0”)

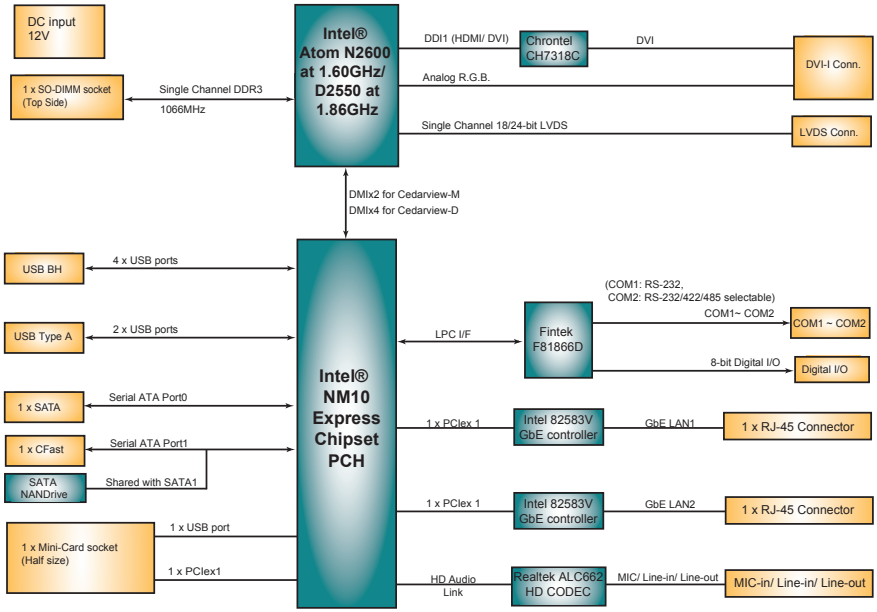
1.11 Board Dimensions



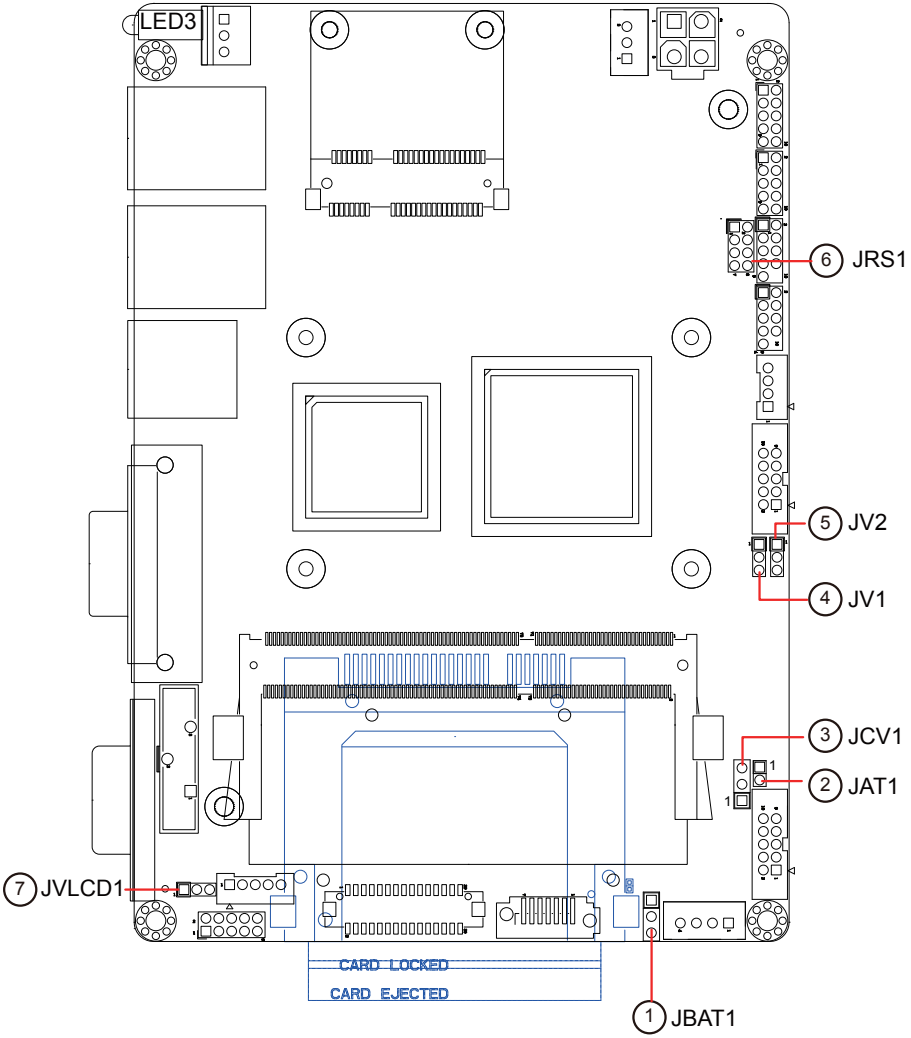
Chapter 2

Installation

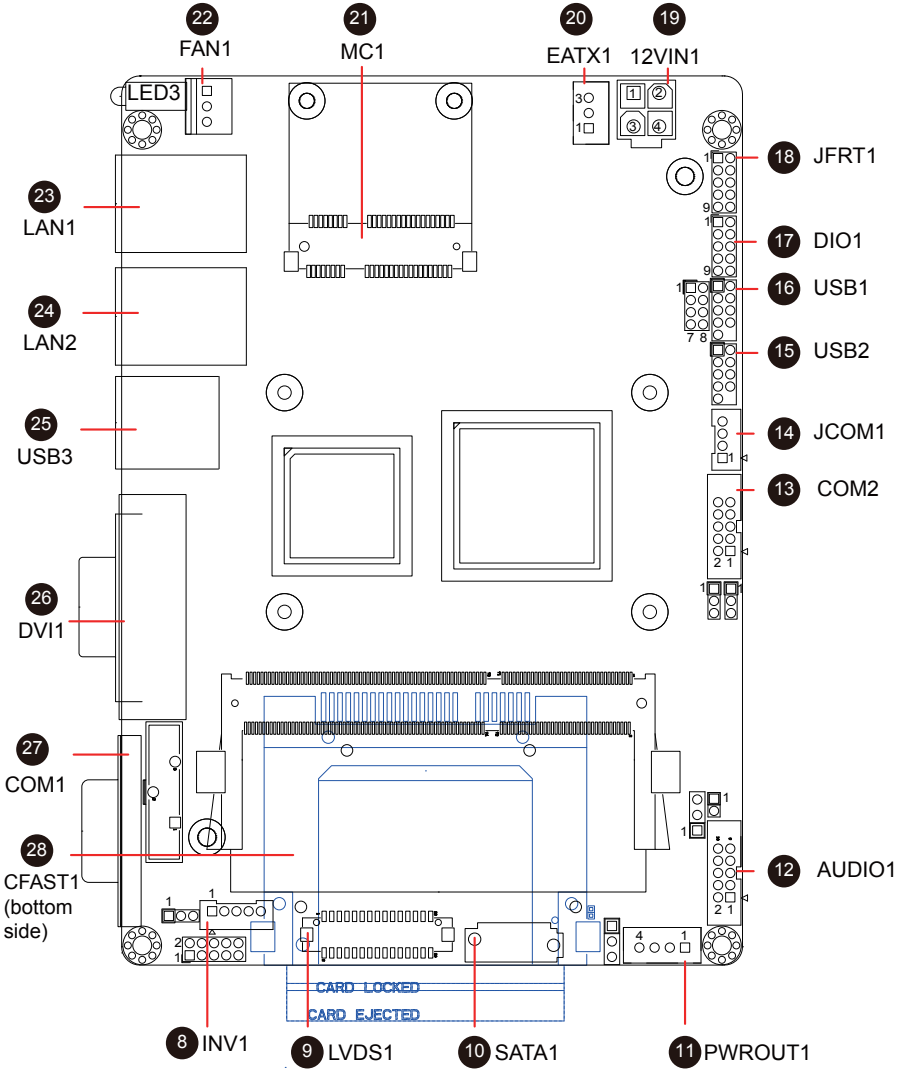
2.1 Block Diagram



2.2 Jumpers


LED3
6 JRS1
5 JV2
4 JV1
3 JCV1
2 JAT1
7 JVLCD1
CARD LOCKED
CARD EJECTED
1 JBAT1

2.3 Connectors



Jumpers

JBAT1: Clear CMOS Setting (1)

If the board refuses to boot due to inappropriate CMOS settings here is how to proceed to clear (reset) the CMOS to its default values.
Connector type: 2.54mm pitch 1x3-pin headers

Pin	Mode	
1-2	Keep CMOS (Default)	
2-3	Clear CMOS	

You may need to clear the CMOS if your system cannot boot up because you forgot your password, the CPU clock setup is incorrect, or the CMOS settings need to be reset to default values after the system BIOS has been updated. Refer to the following solutions to reset your CMOS setting:

Solution A:

1. Power off the system and disconnect the power cable.
2. Place a shunt to short pin 2 and pin 3 of JBAT1 for five seconds.
3. Place the shunt back to pin 1 and pin 2 of JBAT1.
4. Power on the system.

Solution B:

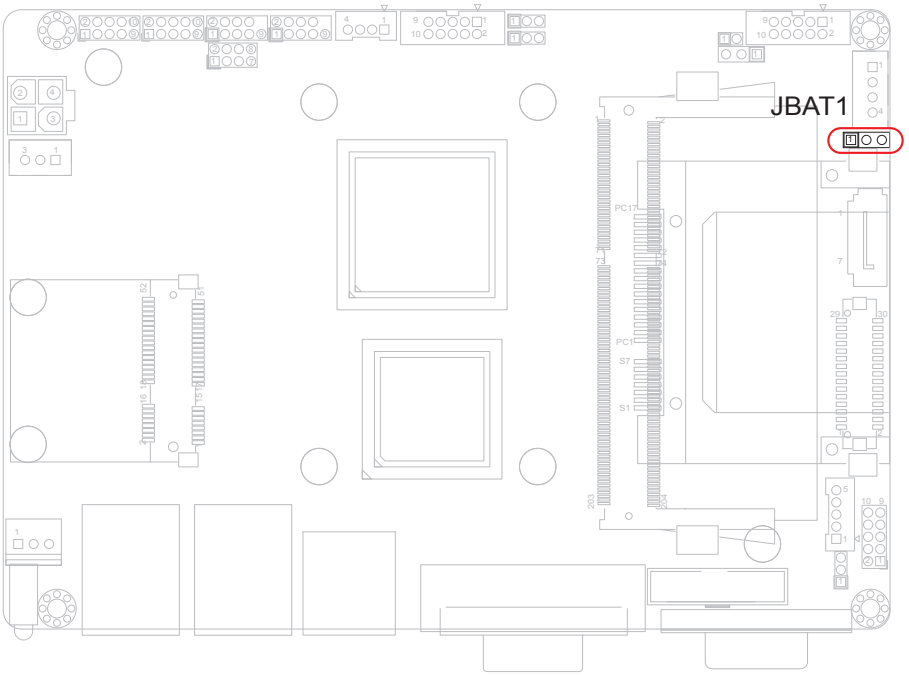
If the CPU Clock setup is incorrect, you may not be able to boot up. In this case, follow these instructions:

Turn the system off, then on again. The CPU will automatically boot up using standard parameters.

As the system boots, enter BIOS and set up the CPU clock.

Note:

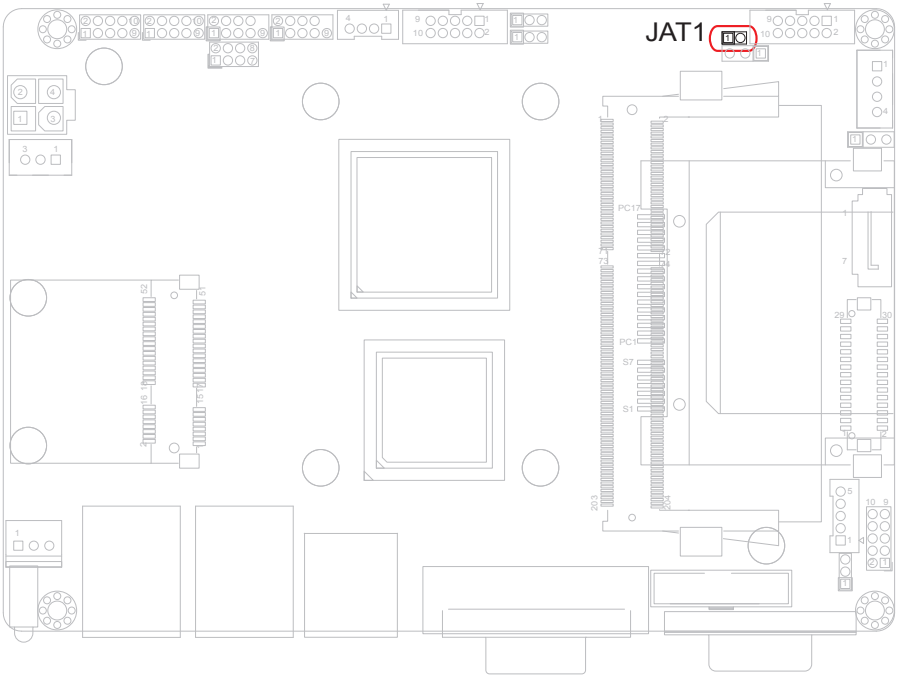
If you are unable to enter BIOS setup, turn the system on and off a few times.


JBAT1

JAT1: AT/ATX Power Mode Selection (2)

The power mode jumper selects the power mode for the system.
Connector type: 2.00mm pitch 1x2-pin headers.

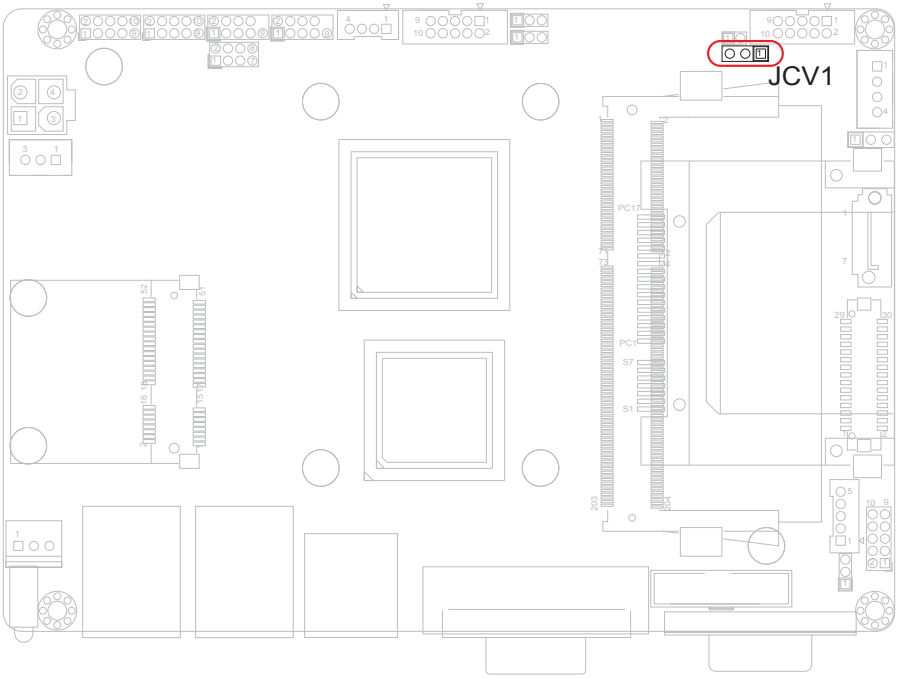
Pin	Mode	
Short	AT Mode	
Open	ATX Mode (Default)	



JCV1: COM Port Power Selector (3)

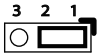
The pin-9 of COM1 and COM2 ports could be selected to +5V or +12V.
Connector type: 2.54mm pitch 1x3-pin headers.

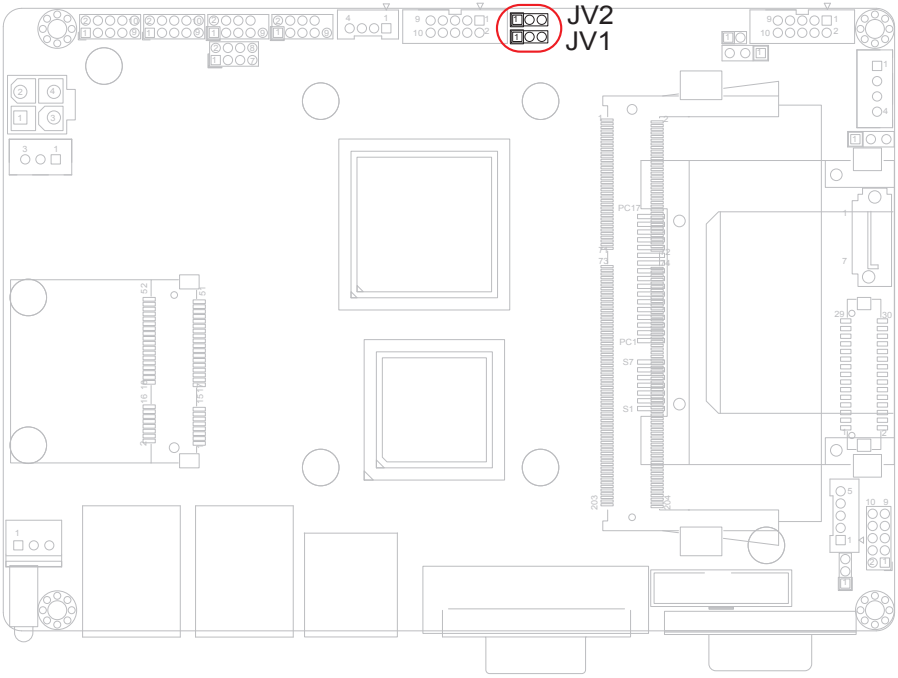
Pin	Mode	
1-2	+5V (Default)	
2-3	+12V	



JV1/ JV2: Voltage/ RI Selector for COM1/ COM2 (4, 5)

The pin-9 of COM1 and COM2 ports could be selected to +5V or +12V by JCV1 and be selected to RI by JV1/ JV2.
Connector type: 2.54mm pitch 1x3-pin headers.

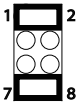
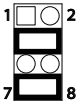
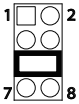
Pin	Mode	
1-2	RI (Default)	
2-3	+5V/+12V (depends on JCV1)	



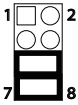
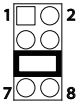
JRS1: COM2 RS-232/422/485 Mode Selection (6)

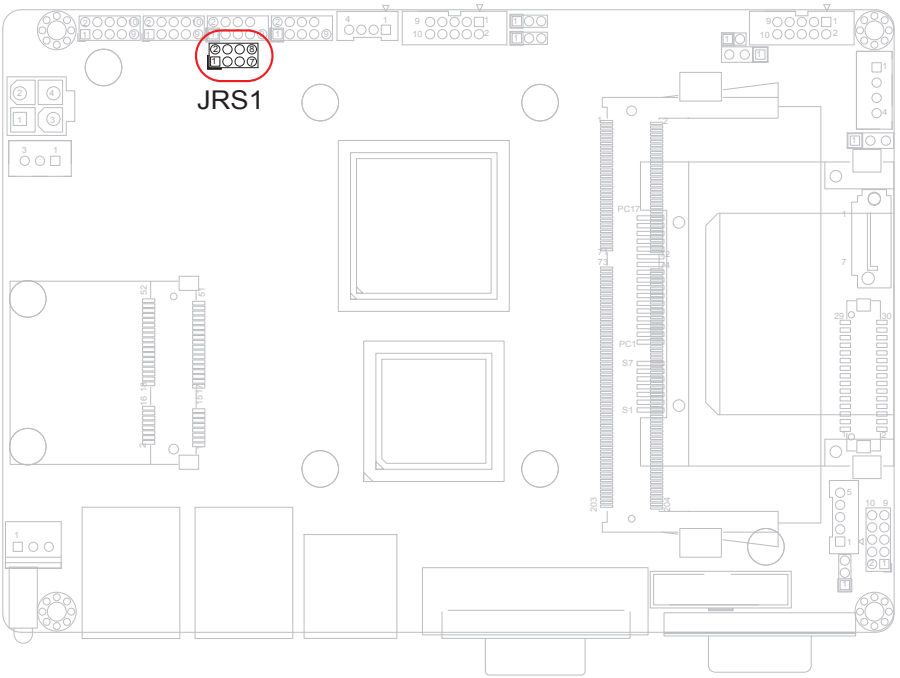
The onboard COM2 port can be configured to operate in RS-422 or RS-485 modes. RS-422 modes differ in the way RX/TX is being handled. Jumper JRS1 switches between RS-232 or RS-422/485 mode. All RS-232/422/482 modes are available on COM2.

Connector type: 2.00mm pitch 2x4-pin headers.

Mode	RS-232 (Default)	RS-422	RS-485
1-2	Short	Open	Open
3-4	Open	Short	Open
5-6	Open	Open	Short
			

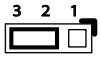
JRS1: COM2 RS-485 Auto-FLow Selection (6)

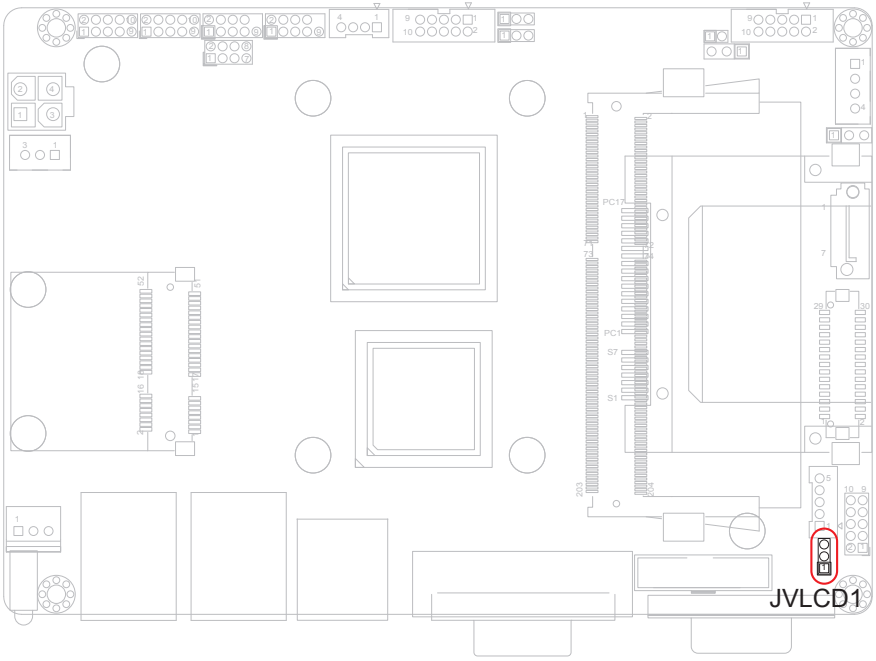
Mode	Disable	Enable
5-6	Short	Short
7-8	Short	Open
		


JRS1

JVLCD1: LVDS1 LCD Panel Voltage Selection (7)

The voltage of LCD panel could be selected by JVLCD1 in +5V or +3.3V.
Connector type: 2.00 mm pitch 1x3-pin headers

Pin	Voltage	
1-2	+5V	
2-3	+3.3V (Default)	

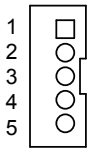


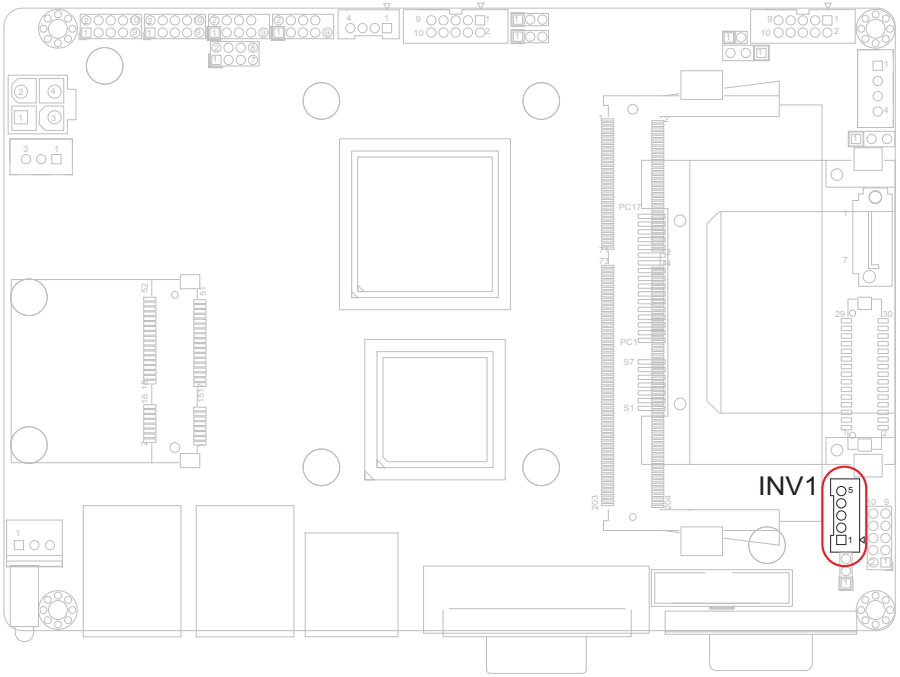
Connectors

INV1: LCD Inverter Connector (8)

Connector type: 2.00mm pitch 1x5-pin box wafer connector.

Pin	Description
1	+12V
2	GND
3	on/off
4	Brightness control
5	GND

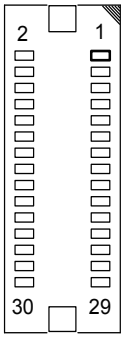


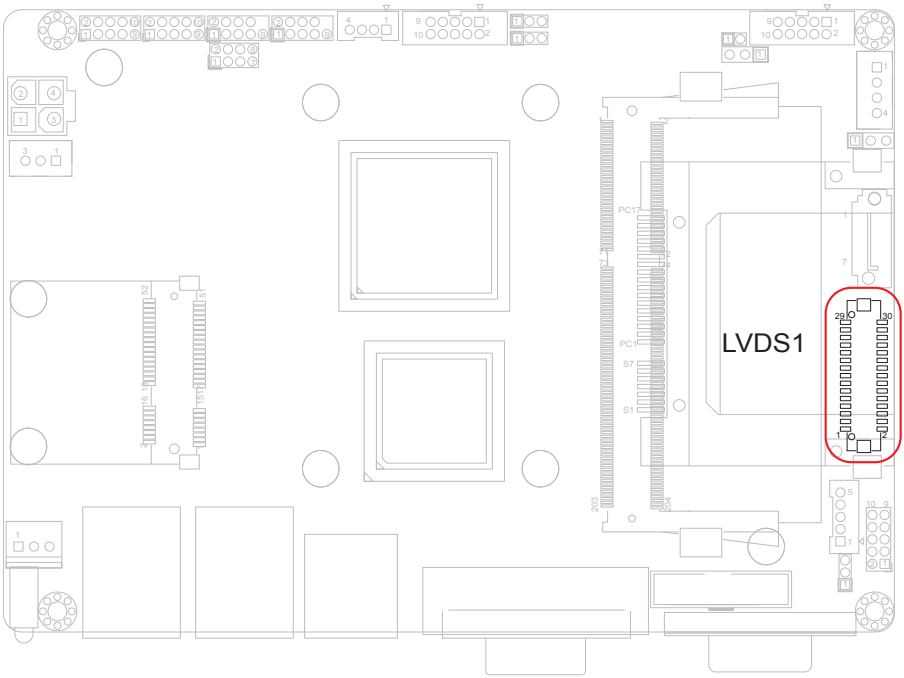


LVDS1: LVDS Connector (9)

The LVDS connector supports single channel 18-bit or 24-bit LVDS. VDD could be selected by JVLCD1 in +5V or +3.3V.
Connector type: DF-13-30DP-1.25V

Pin	Description	Pin	Description
2	VDD	1	VDD
4	N/C	3	TX1_CLK+
6	N/C	5	TX1_CLK-
8	GND	7	GND
10	N/C	9	TX1_D0+
12	N/C	11	TX1_D0-
14	GND	13	GND
16	N/C	15	TX1_D1+
18	N/C	17	TX1_D1-
20	GND	19	GND
22	N/C	21	TX1_D2+
24	N/C	23	TX1_D2-
26	GND	25	GND
28	N/C	27	TX1_D3+
30	N/C	29	TX1_D3-

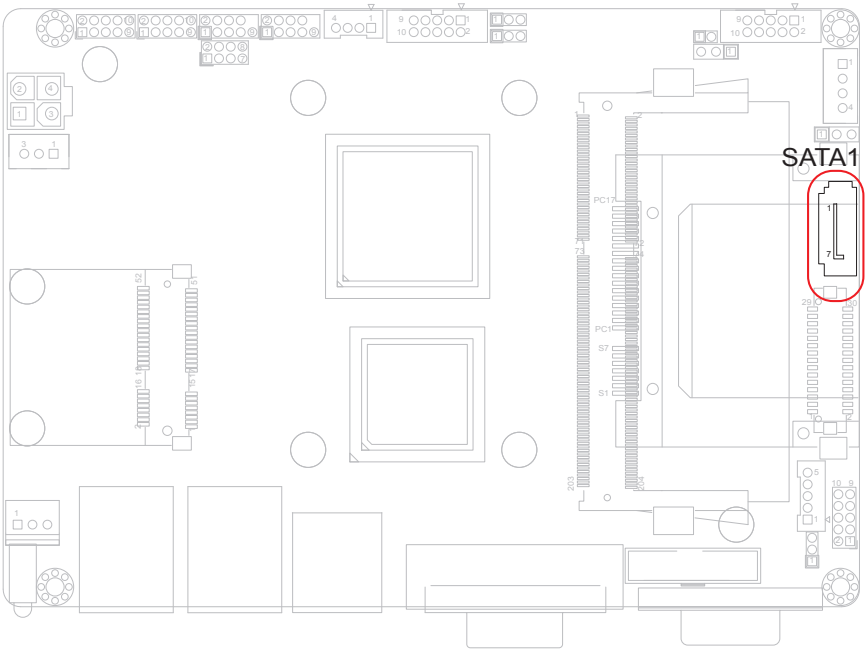



LVDS1

SATA1: Serial ATA Connector (10)

There are on board two SATA connectors, third generation SATA drives transfer data at speeds as high as 600MB/s, twice the transfer speed of first generation SATA drives.

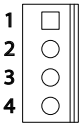
Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

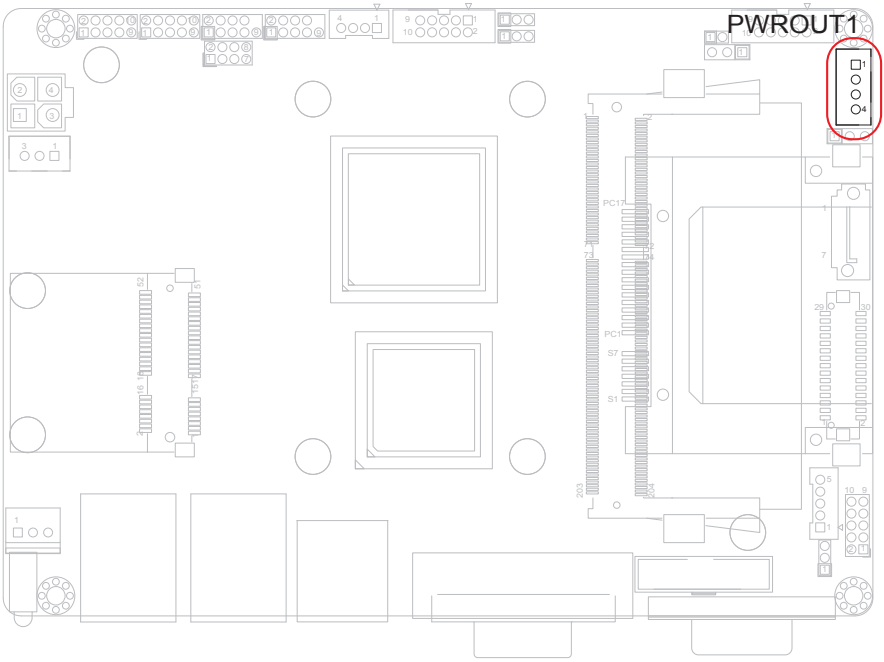


PWROUT1: SATA Power Connector (11)

Connector type: 2.54mm pitch 1x4-pin wafer one wall connector

Pin	Description
1	+5V
2	GND
3	GND
4	+12V

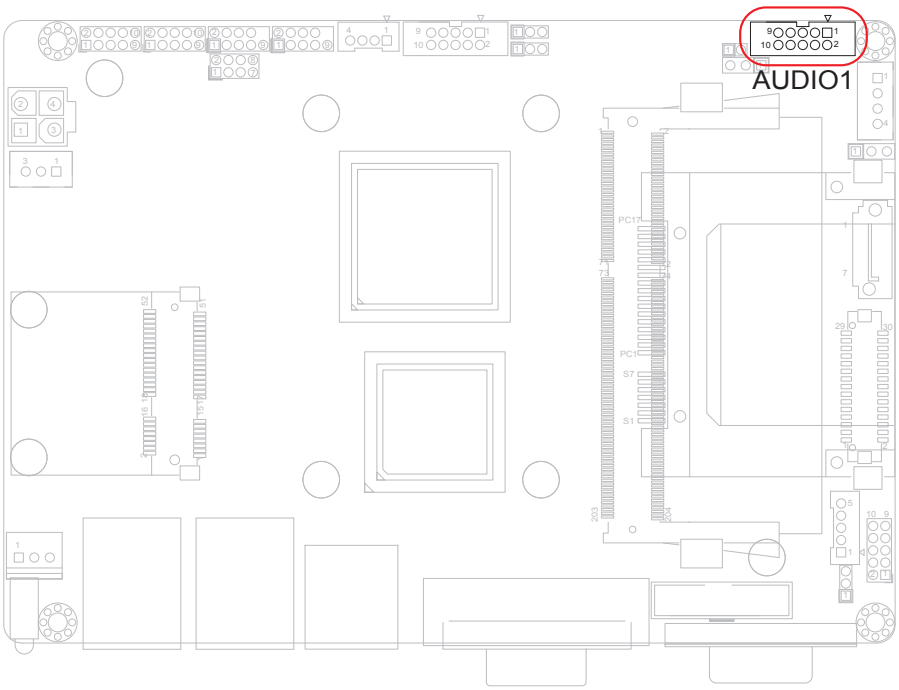




AUDIO1: AUDIO Connector (12)

Connector type: 2.00mm pitch 2x5-pin box header.

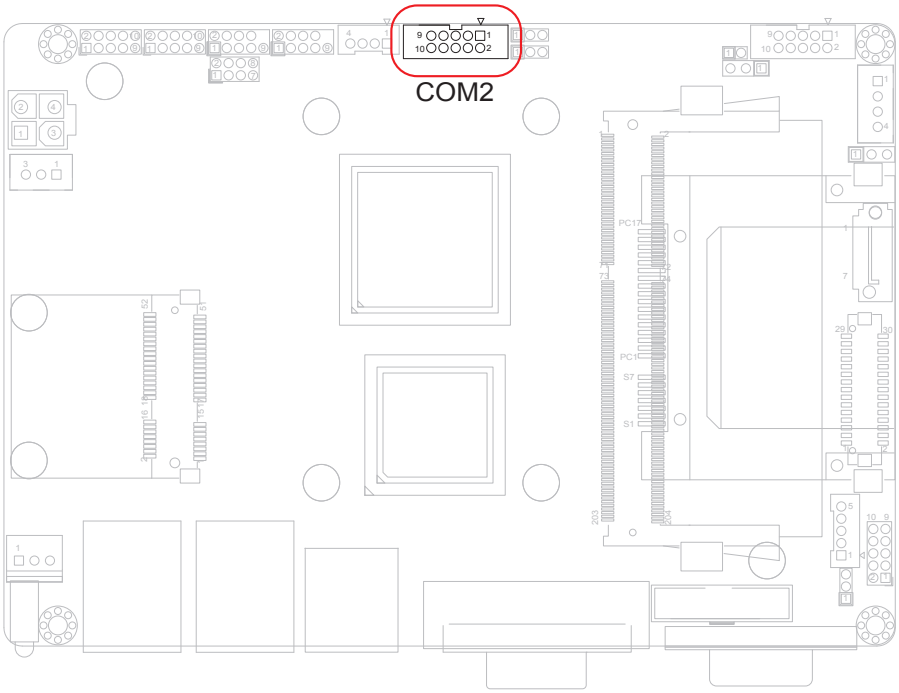
Pin	Description	Pin	Description
1	Lin_In_Left	2	Line_In_Right
3	GND	4	GND
5	MICL	6	MICR
7	GND	8	GND
9	Speaker Left	10	Speaker Right



COM2: Serial Port Connector (13)

Connector type: 2.00mm pitch 2x5-pin box header.

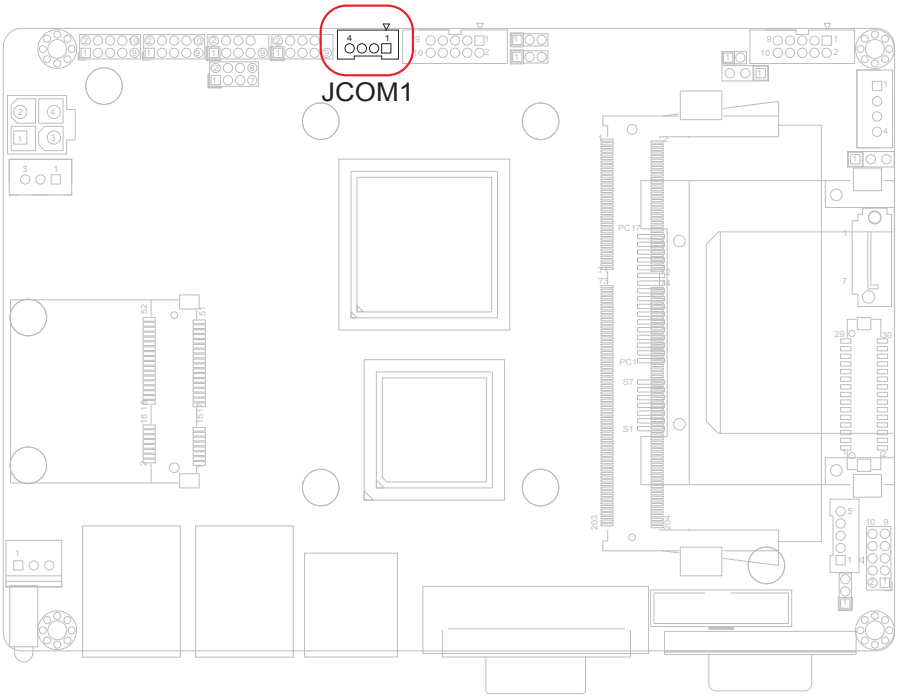
Pin	Description	Pin	Description
1	DCD#2	2	RXD2
3	TXD2	4	DTR#2
5	GND	6	DSR#2
7	RTS#2	8	CTS#2
9	RI2	10	N/C



JCOM1: COM2 RS-422/ 485 Connector (14)

Connector type: 2.00mm pitch 1x4 box wafer connector

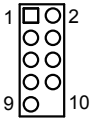
Pin	RS-422	RS-485
1	TX+	Data+
2	TX-	Data-
3	RX+	N/C
4	RX-	N/C

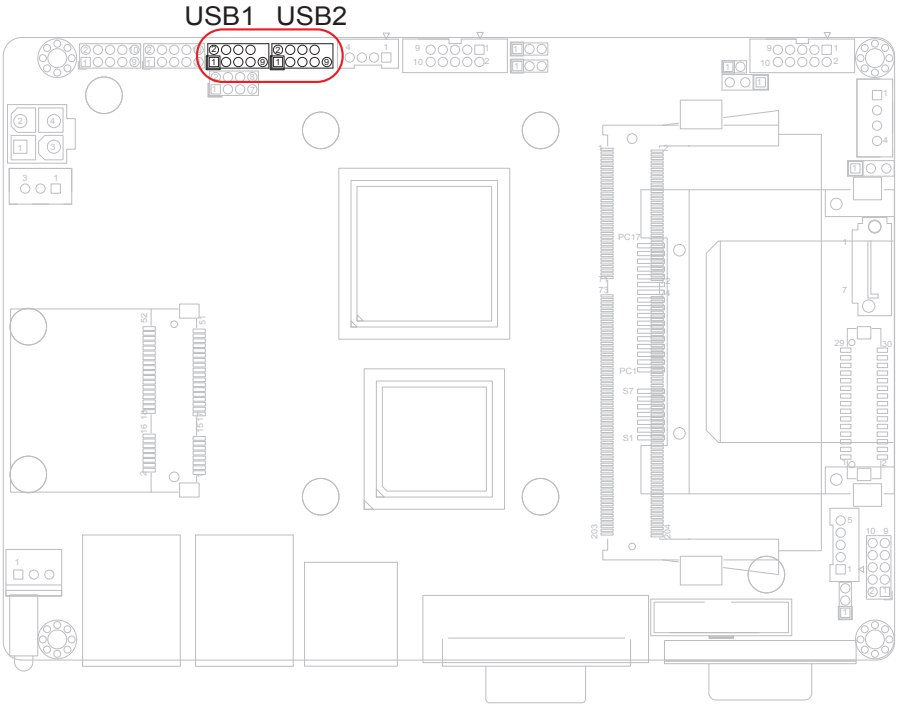


USB1, 2: USB Connectors (15, 16)

The CPU board on board supports two headers USB1, USB2 that can connect up to 4 high-speed (Data transfers at 480Mb/s), full-speed (Data transfers at 12Mb/s) or low-speed (Data transfers at 1.5Mb/s) USB devices.
Connector type: 2.00mm 2x5-pin headers

Pin	Description	Pin	Description
1	+5V	2	+5V
3	USBD-	4	USBD-
5	USBD+	6	USBD+
7	GND	8	GND
9	N/C	10	N/C (Key)

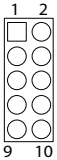


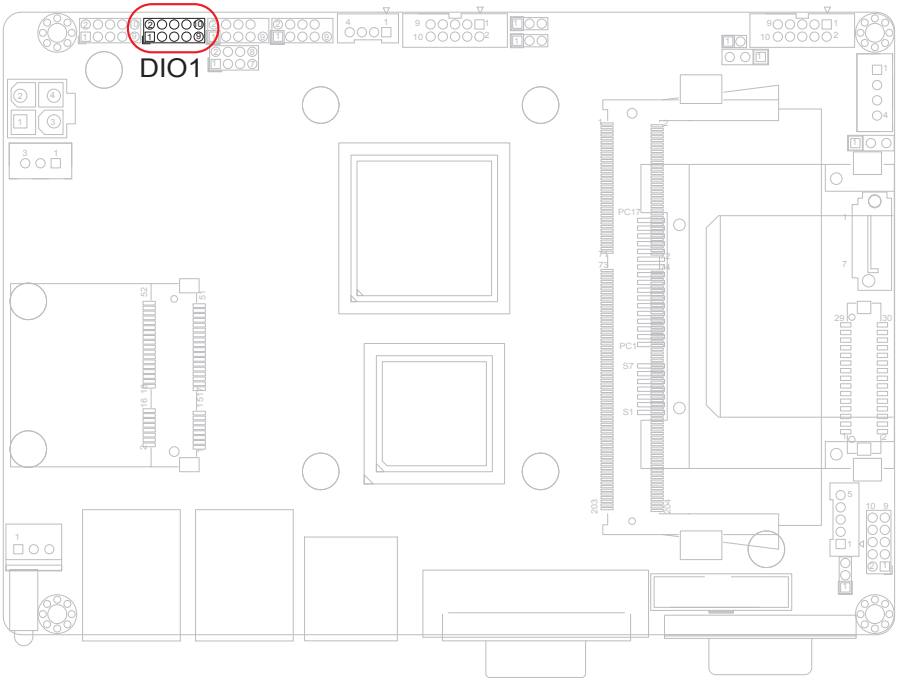


DIO1: Digital I/O Connector (17)

DIO1 is a 8-bit DIO connector that supports 8-bit programmable digital Input and Output.
Connector type: 2.00 mm pitch 2x5-pin headers.

Pin	Description	Pin	Description
1	DIO1	2	DIO2
3	DIO3	4	DIO4
5	DIO5	6	DIO6
7	DIO7	8	DIO8
9	+5V	10	GND

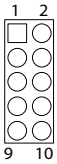




JFRT1: Switches and Indicators (18)

It provides connectors for system indicators that provides light indication of the computer activities and switches to change the computer status.
Connector type: 2.00 mm pitch 2x5-pin headers

Pin	Description	Pin	Description
1	RESET+	2	RESET-
3	POWER_LED+	4	POWER_LED-
5	HDD_LED+	6	HDD_LED-
7	SPEAK+	8	SPEAK-
9	PWRBTN+	10	PWRBTN-



RESET: Reset Button, pin 1-2.

This 2-pin connector connects to the case-mounted reset switch and is used to reboot the system.

POWER_LED: Power LED Connector, pin 3-4.

This 2-pin connector connects to the case-mounted power LED. Power LED can be indicated when the CPU card is on or off. And keyboard lock can be used to disable the keyboard function so the PC will not respond by any input.

HDD_LED: HDD LED Connector, pin 5-6.

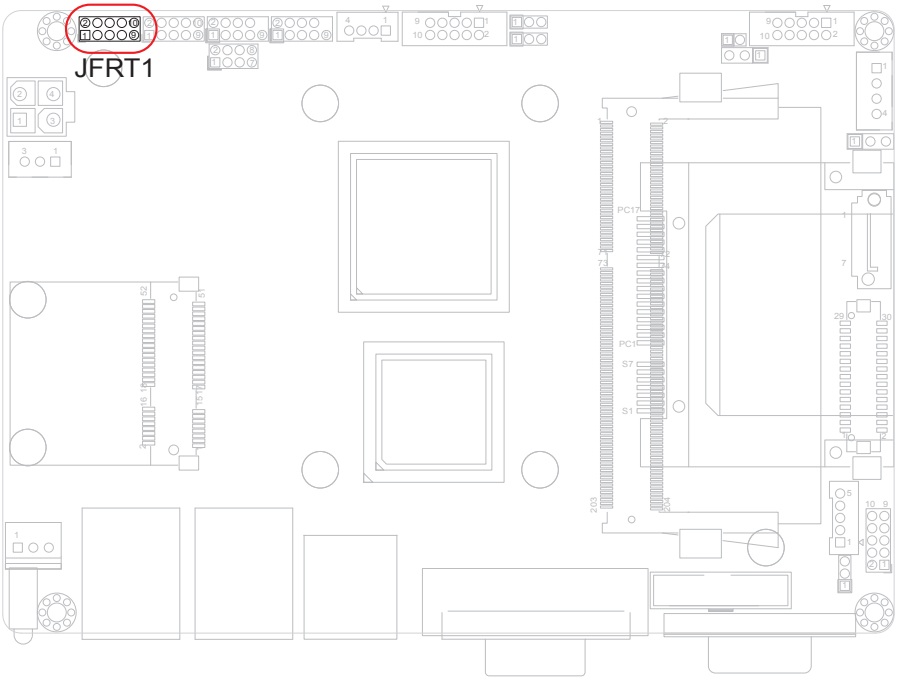
This 2-pin connector connects to the case-mounted HDD LED to indicate hard disk activity.

SPEAK: External Speaker, pin 7-8.

This 2-pin connector connects to the case-mounted speaker.

PWRBTN: ATX soft power switch, pin 9-10.

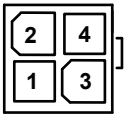
This 2-pin connector connects to the case-mounted Power button.

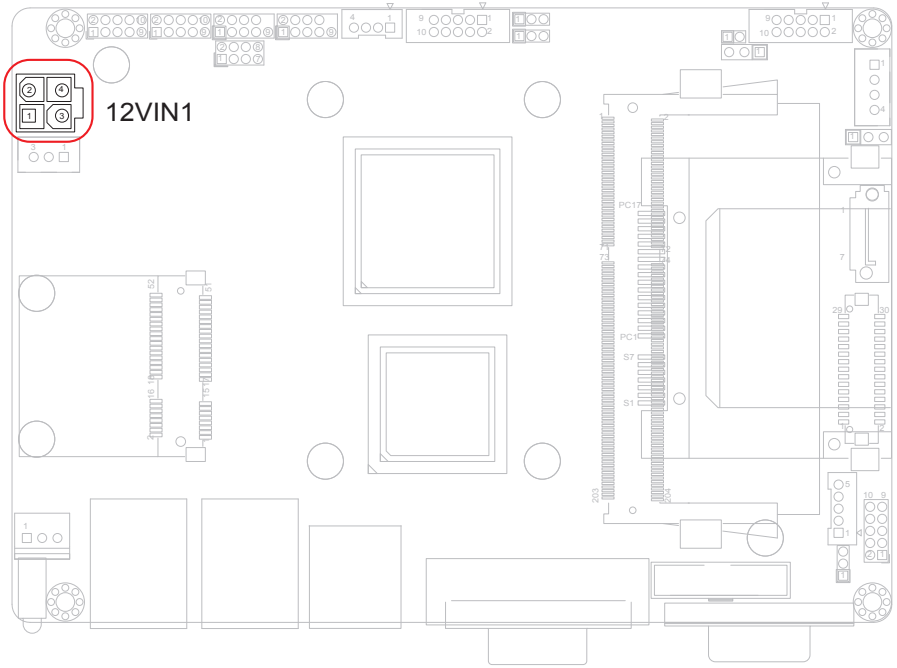

JFRT1

12VIN1: ATX +12V Connector (19)

PWR1 supplies the CPU operation at +12V (Vcore).

Pin	Description	Pin	Description
2	GND	4	+12V
1	GND	3	+12V

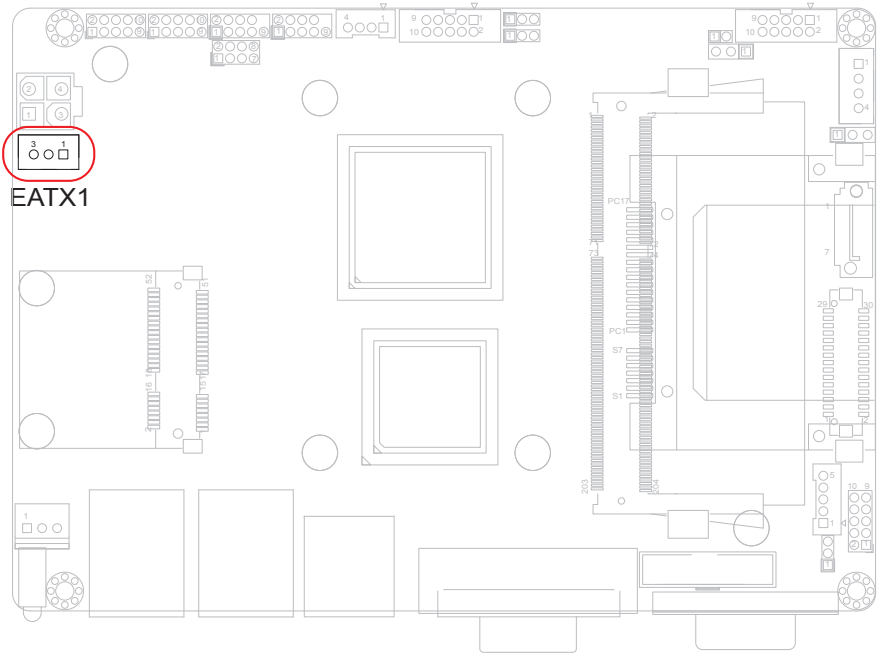




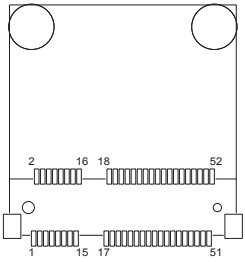
EATX1: ATX Feature Connector (20)

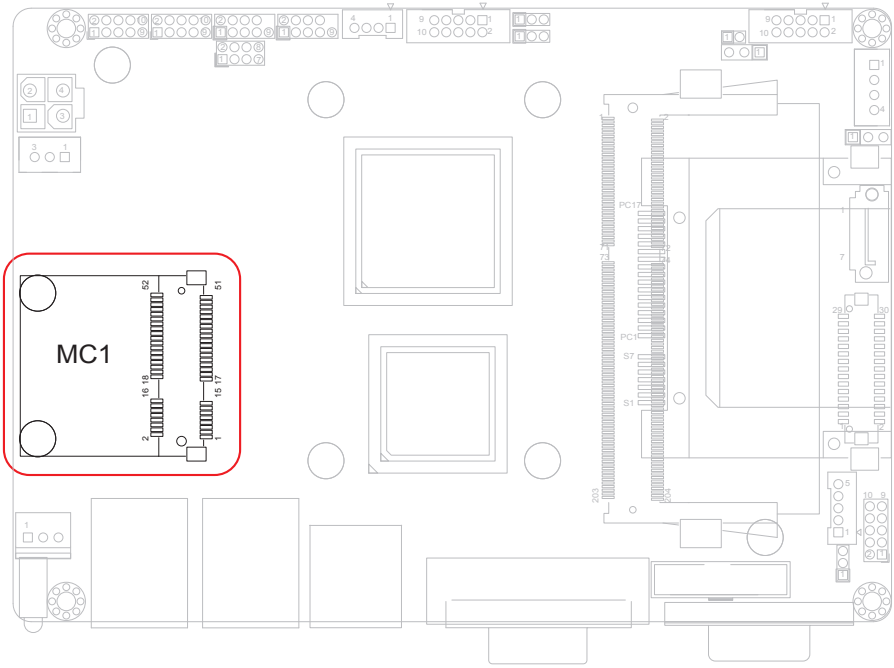
Connector type: 2.54mm pitch 1x3-pin box wafer connector

Pin	Description
1	PS-ON
2	GND
3	5V_SB



MC1: Mini-card Socket (21)

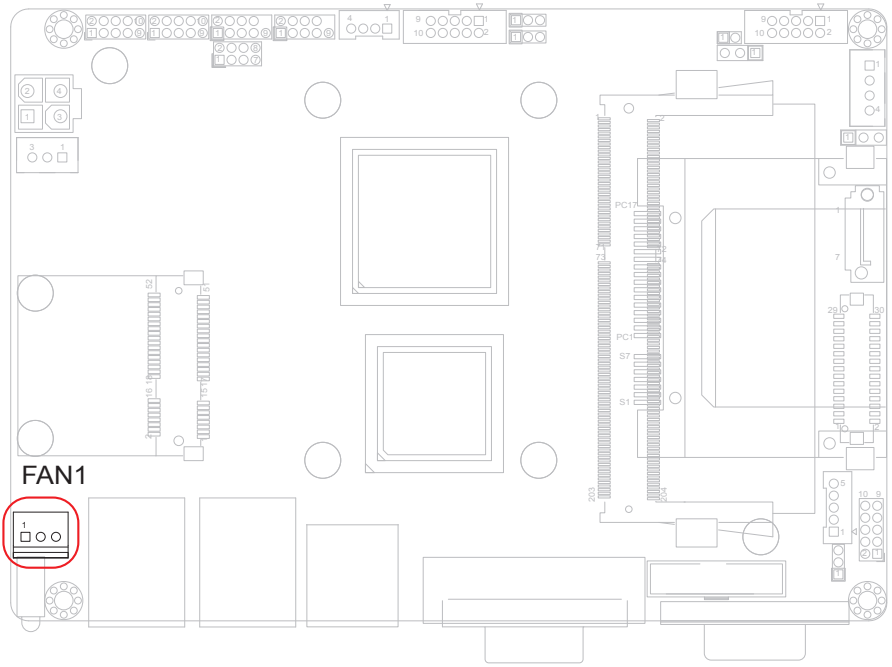




FAN1: CPU Fan Connector (22)

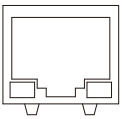
FAN1 is a 3-pin header for the CPU fan. The fan must be a +12V fan.

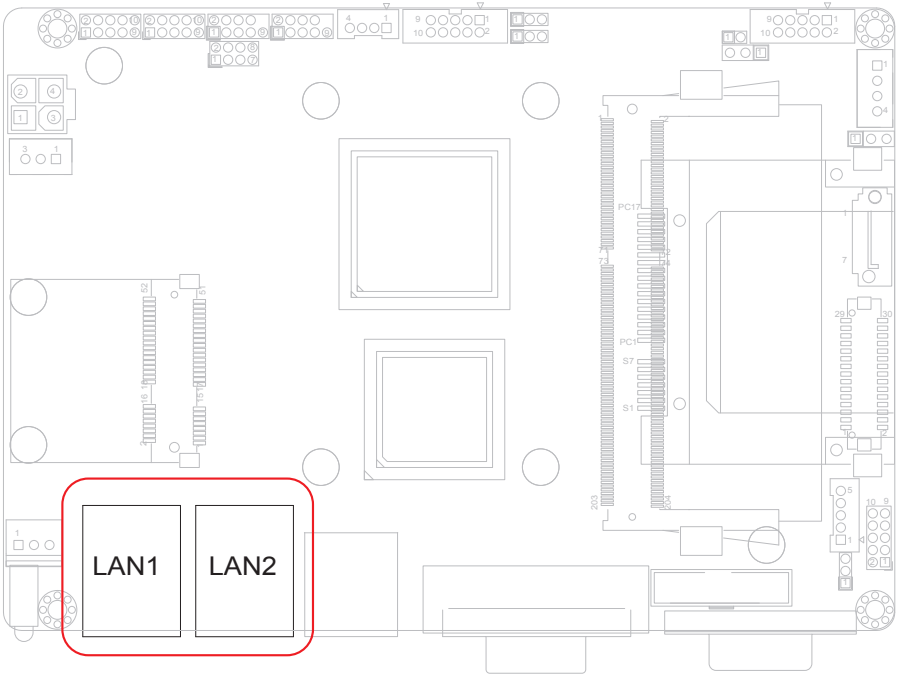
Pin	Description
1	GND
2	+12V
3	FAN Speed



LAN1, 2: Gigabit Ethernet Connectors (23, 24)

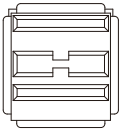
These connectors support Gigabit Ethernet.

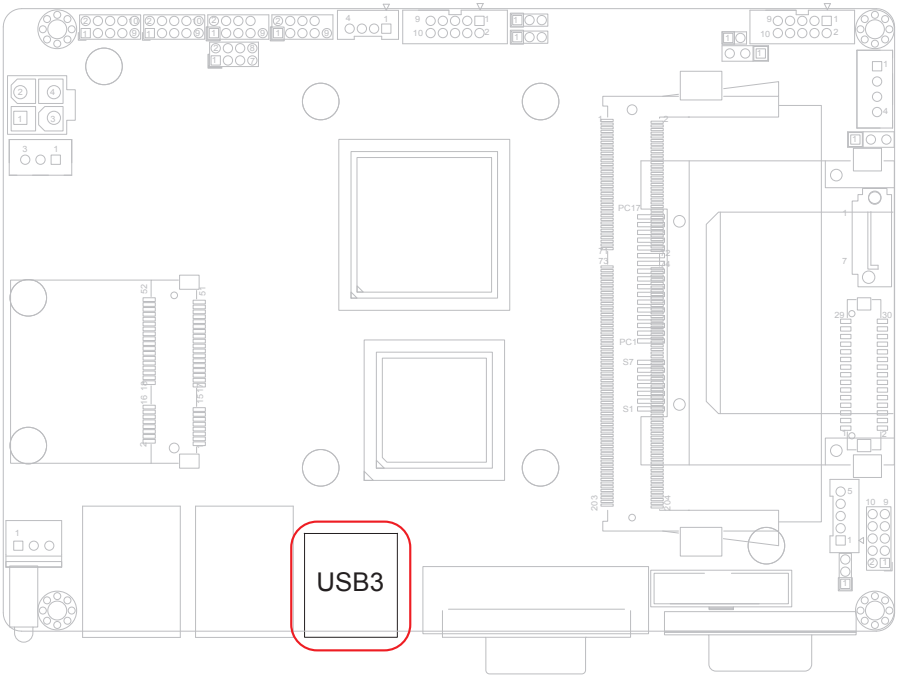




USB3: USB Port Connectors (25)

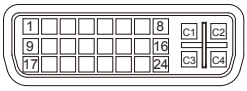
Connector type: double stack USB type A.





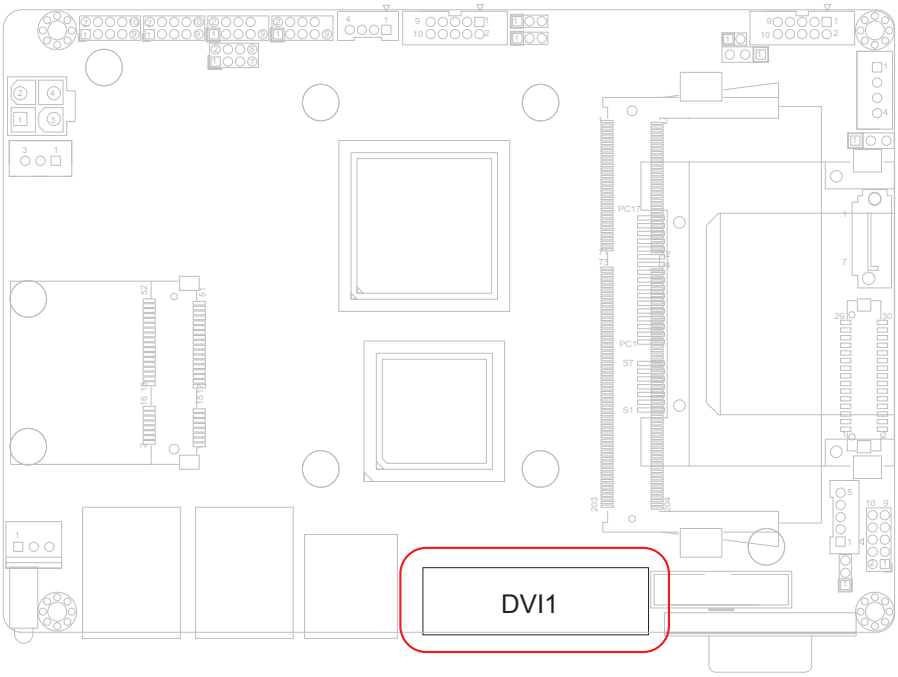
DVI1: DVI Connector (26)

Connector type: DVI-I female.



DVI-I Connector

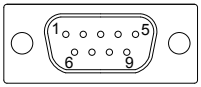
Pin	Description	Pin	Description	Pin	Description
1	DATA2-	9	DATA1-	17	DATA0-
2	DATA2+	10	DATA1+	18	DATA0+
3	DATA 2/4 SHIELD	11	DATA 1/3 SHIELD	19	DATA 0/5 SHIELD
4	DATA 4- (LINK 1, NC	12	DATA 3- (LINK 1, NC	20	DATA 5- (LINK 1, NC
5	DATA 4+ (LINK 1, NC)	13	DATA 3+ (LINK 1, NC)	21	DATA 5+ (LINK 1, NC)
6	DDC_CLK	14	+5V	22	Clock_SHIELD
7	DDC_DATA	15	GND (for +5V)	23	Clock+
8	VGA_V_Sync	16	Hot Plug Detect	24	Clock-
C1 VGA Red					
C2 VGA Green					
C3 VGA Blue					
C4 VGA_H_Sync					
C5 VGA_R,G,B_Return					

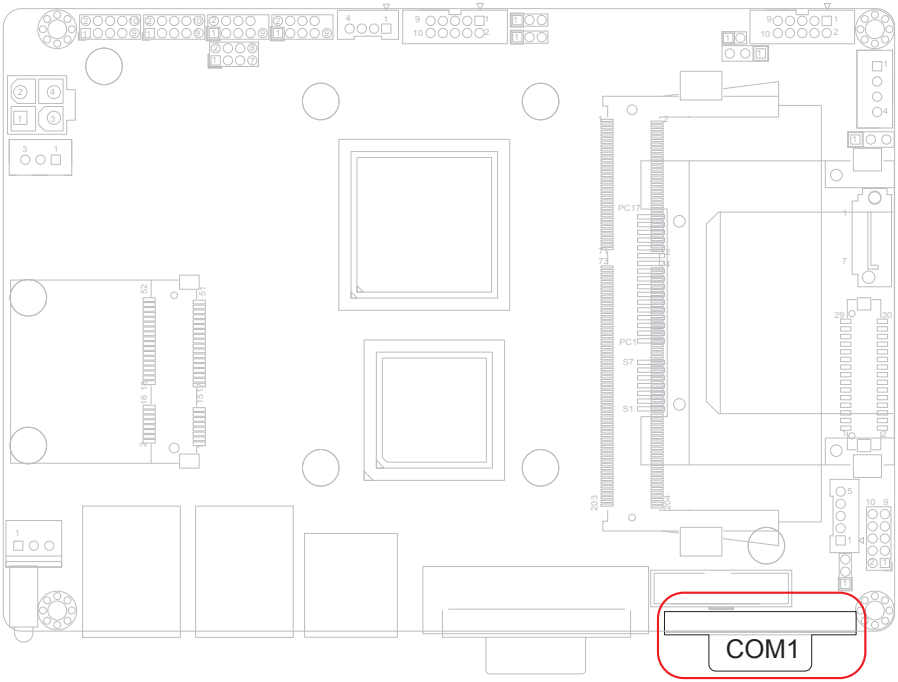

DVI1

COM1: Serial Port Connector (27)

Connector type: D-Sub 9-pin male.

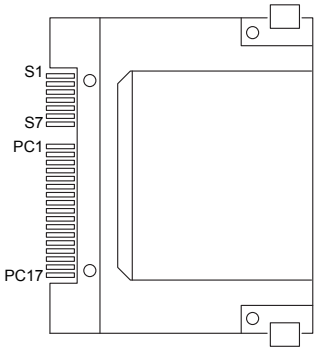
Pin	Description	Pin	Description
1	DCD#1	6	DSR#1
2	RXD1	7	RTS#1
3	TXD1	8	CTS#1
4	DTR#1	9	RI1
5	GND		

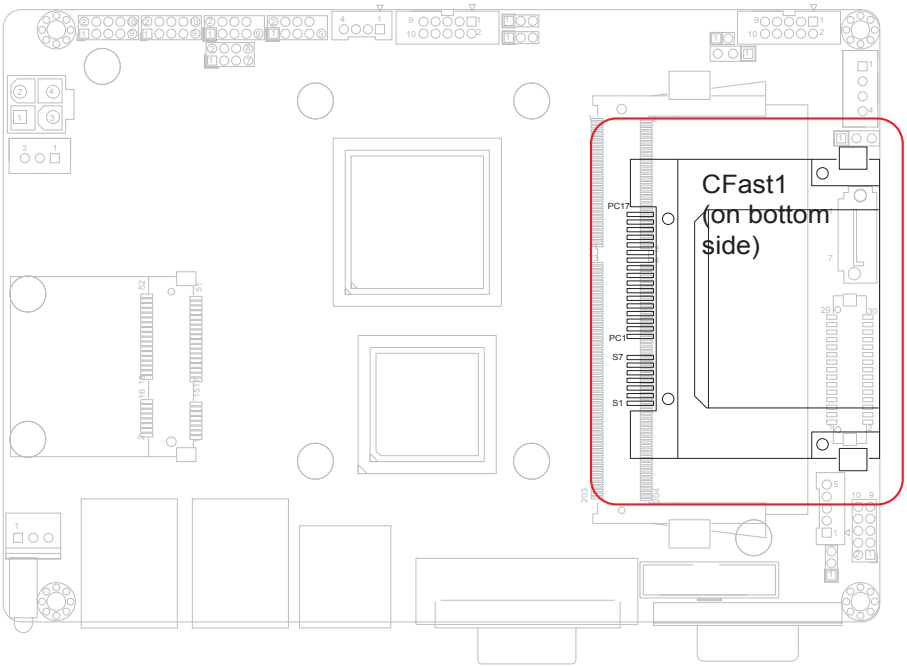




CFast1: CFast Socket (28, battom side)

Pin	Description
S1	SGND1
S2	TXP
S3	TXN
S4	SGND2
S5	RXN
S6	RXP
S7	SGND
PC1	CDI
PC2	GND
PC3	TBD
PC4	TBD
PC5	TBD
PC6	TBD
PC7	GND
PC8	LED1
PC9	LED2
PC10	IO1
PC11	IO2
PC12	IO3
PC13	3.3V
PC14	3.3V
PC15	GND
PC16	GND
PC17	CD0




CFast1
(on bottom
side)
PC17
PC1
S7
S1

2.4 The Installation Paths of CD Driver

Windows 7

Driver	Path
CHIPSET	\EmETXe-i250x\CHIPSET\WIN7
VGA	\EmETXe-i250x\GRAPHICS
AUDIO	\EmETXe-i250x\AUDIO
LAN	\EmETXe-i250x\ETHERNET

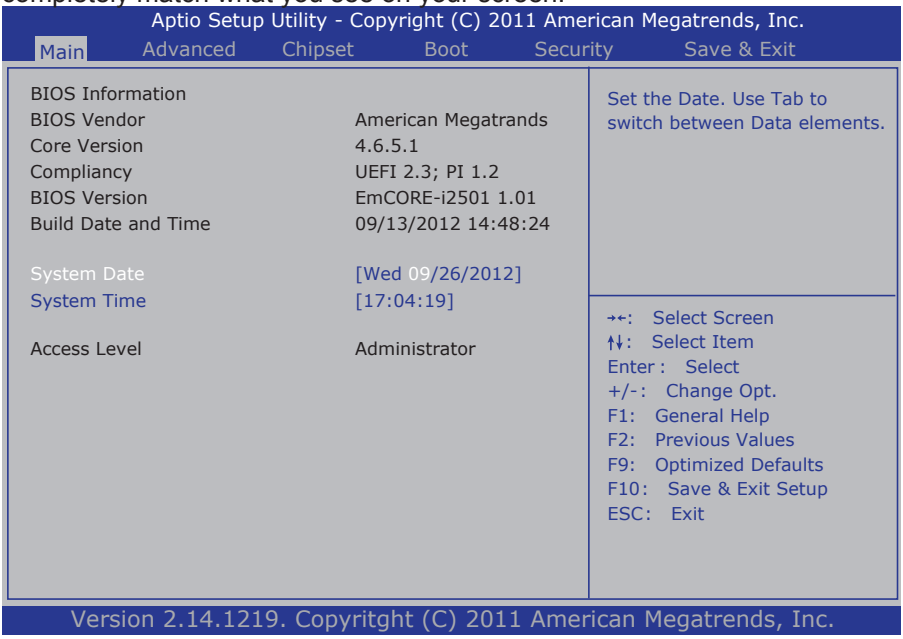
Chapter 3

BIOS

3.1 BIOS Main Setup

The AMI BIOS provides a setup utility program for specifying the system configurations and settings which are stored in the BIOS ROM of the system. When you turn on the computer, the AMI BIOS is immediately activated. After you have entered the setup utility, use the left/right arrow keys to highlight a particular configuration screen from the top menu bar or use the down arrow key to access and configure the information below.

NOTE: In order to increase system stability and performance, our engineering staff are constantly improving the BIOS menu. The BIOS setup screens and descriptions illustrated in this manual are for your reference only, and may not completely match what you see on your screen.



BIOS Information

Display the BIOS information.

System Date

Set the system date. Note that the 'Day' automatically changes when you set the date.

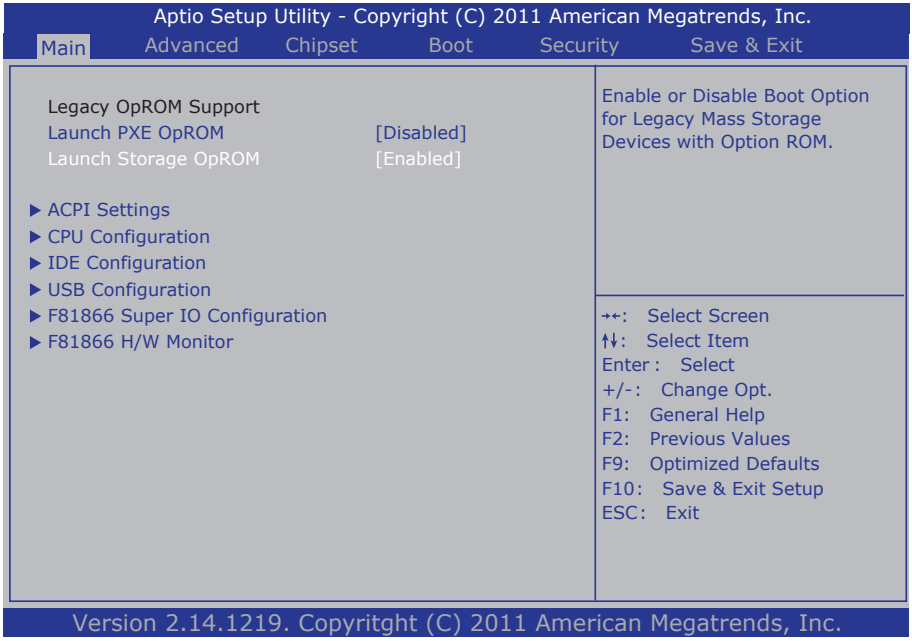
The date format is:

Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1999 to 2099

System Time

Set the system time.
The time format is: **Hour :** 00 to 23
Minute : 00 to 59
Second : 00 to 59

3.2 Advanced Settings



Legacy OpROM Support

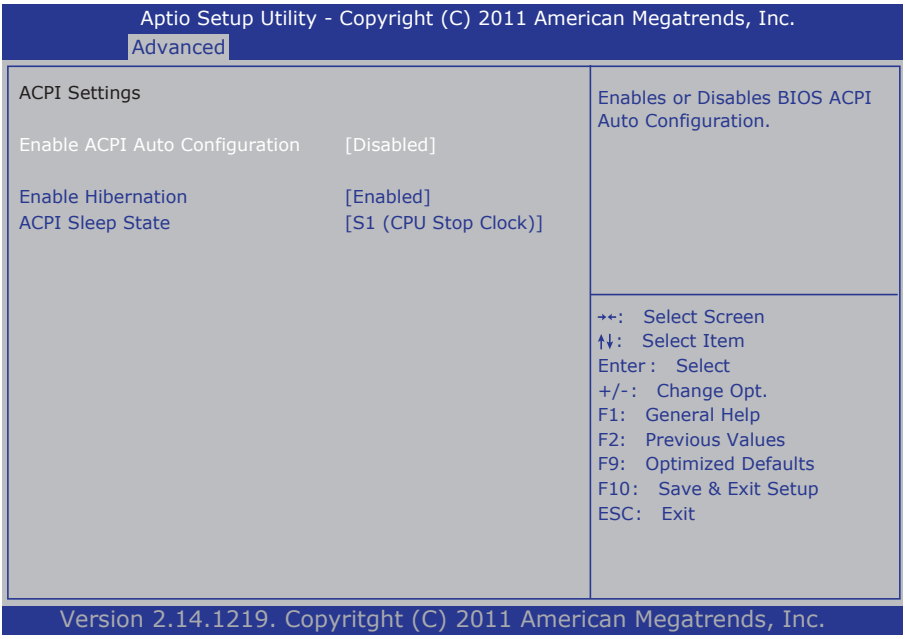
Launch PXE OpROM

Enable or disable the boot option for legacy network devices.

Launch Storage OpROM

Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

3.2.1 ACPI Settings



Enable Hibernation
Enable or disable System ability to Hibernation (OS/S4 Sleep State). This option may be not effective with some OS.

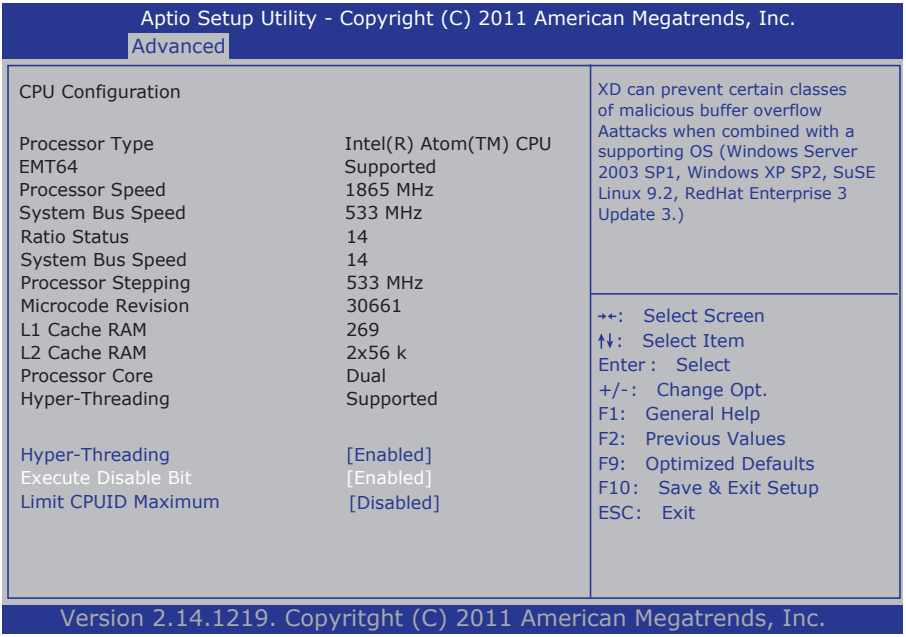
ACPI Sleep State
Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
The choice: Suspend Disabled, S1 (CPU Stop Clock), S3 (Suspend to RAM)

Lock Legacy Resources
Enable or disable Lock of Legacy Resources.

Power-Supply Type
Set power-supply type.
The choice: AT, ATX

3.2.2 CPU Configuration

The CPU Configuration setup screen varies depending on the installed processor.



Hyper-threading

This item is used to enable or disable the processor's Hyper-threading feature.

Enabled for Windows XP and Linux (OS optimized for Hyper-threading Technology) and disabled for other OS (OS not optimized for Hyper-threading Technology).

When disabled, only one thread per enabled core is enabled.

Execute Disable Bit

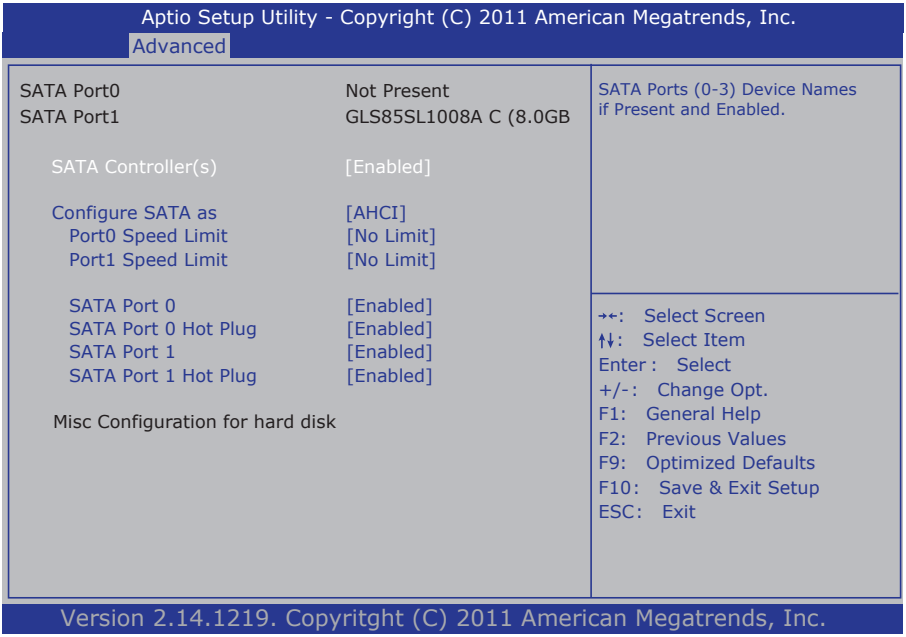
Enable or disable the execute Disable Bit.

Limit CPUID Maximum

Enable or disable the Limit CPUID Maximum.

3.2.3 SATA Configuration

It allows you to select the operation mode for SATA controller.



SATA Controller(s)

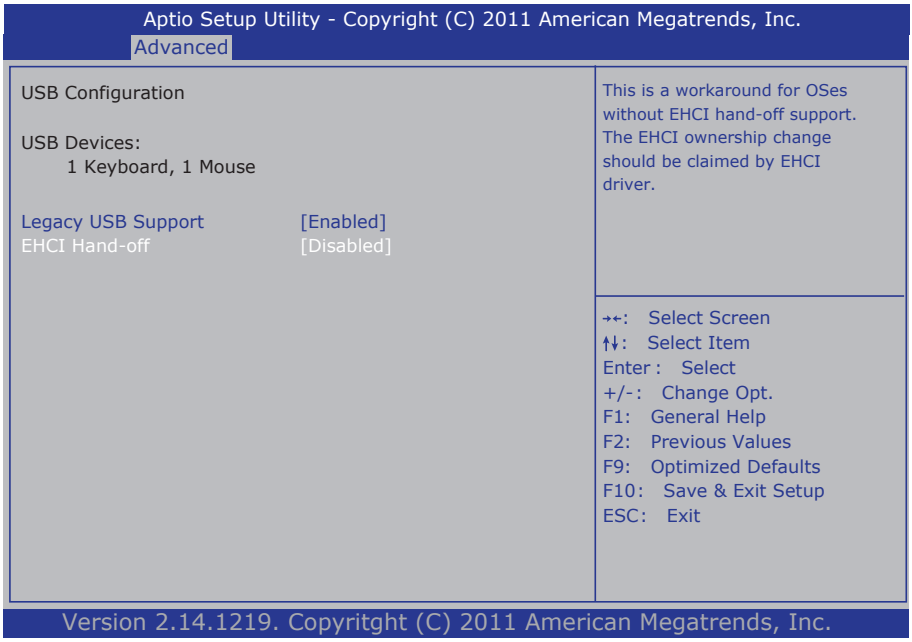
Enable or disable SATA devices.

SATA Mode Selection

The choice: Disable; IDE (Default), AHCI

IDE: Set the Serial ATA drives as Parallel ATA storage devices.
AHCI: Allow the Serial ATA devices to use AHCI (Advanced Host Controller Interface).

3.2.4 USB Configuration



Legacy USB Support

Enable support for legacy USB. AUTO option disables legacy support if no USB devices are connected.
The choice: Enabled (Default); Auto; Disabled

EHCI Hand-off

Allow you to enable support for operating systems without an EHCI hand-off feature. Do not disable the BIOS EHCI Hand-Off option if you are running a Windows® operating system with USB device.
The choice: Enabled (Default); Disabled

USB transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers. Default setting: 20 sec

Device reset time-out

USB mass storage device Start Unit command time-out. Default setting: 20 sec

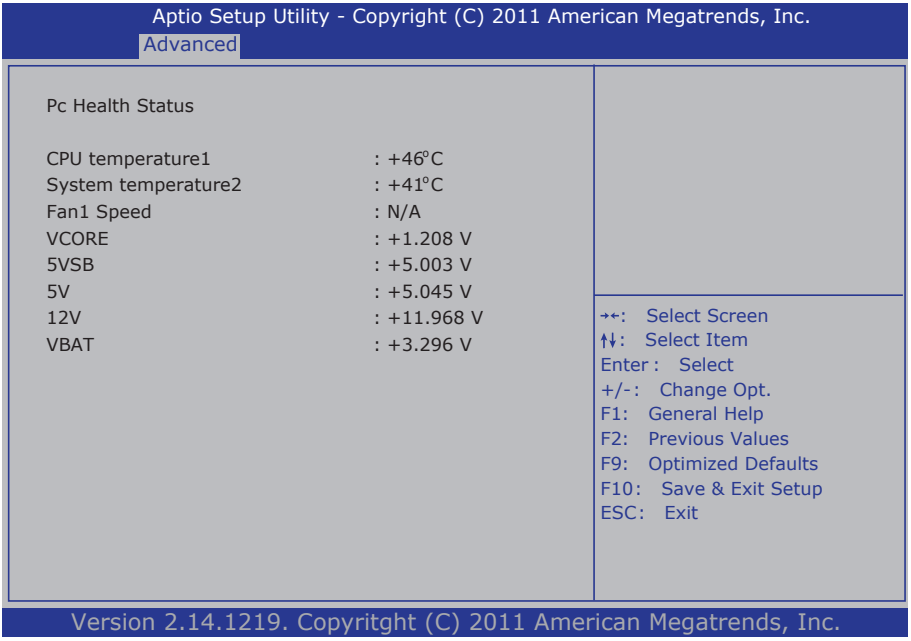
Device power-up delay

Maximum time the device will take before it properly reports itself to the host controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from hub descriptor. The choice: Auto (Default); Manual

Mass Storage Devices

This item displays information when USB devices are detected.

3.2.5 H/W Monitor

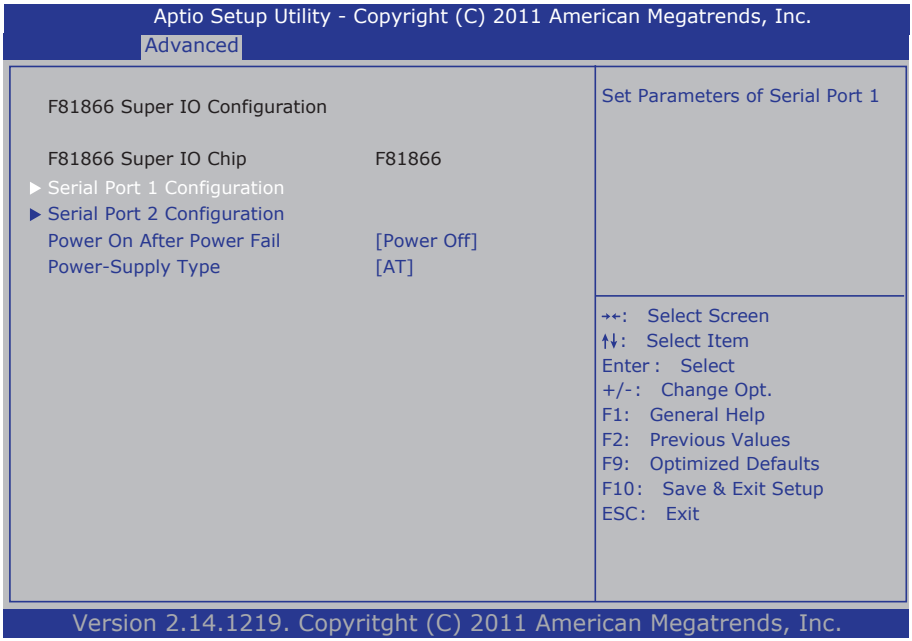


PC Health Status

The hardware monitor menu shows the operating temperature and system voltages of CPU module.

3.2.6 Super IO Configuration

You can use this item to set up or change the Super IO configuration for parallel ports and serial ports.



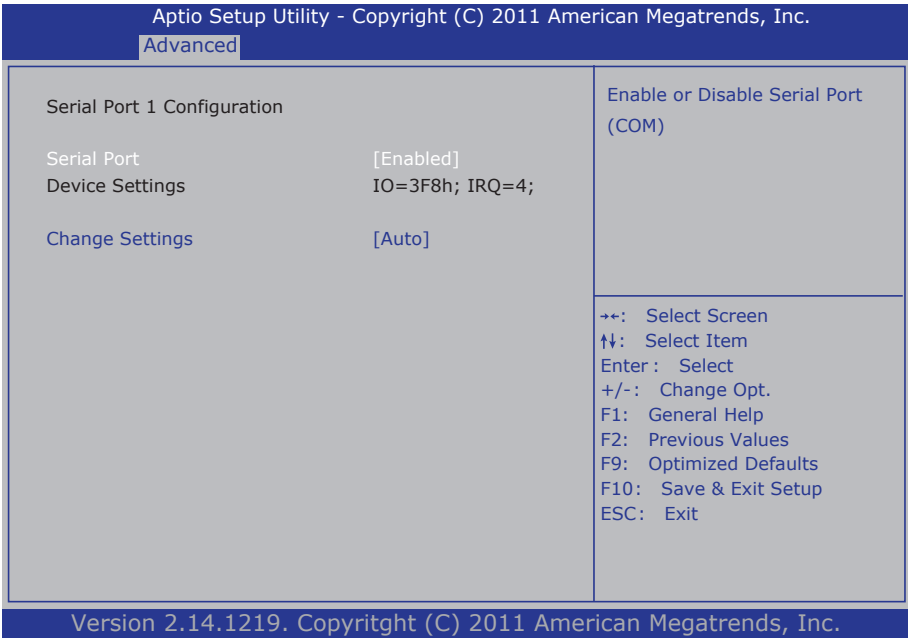
Power On After Power Failure

Specify what state to go to when power is re-applied after a power failure.

Power On by modem Function

Enables or Disables the Power On by modem fuction.

Serial Port 1~2 Configuration



Serial Port

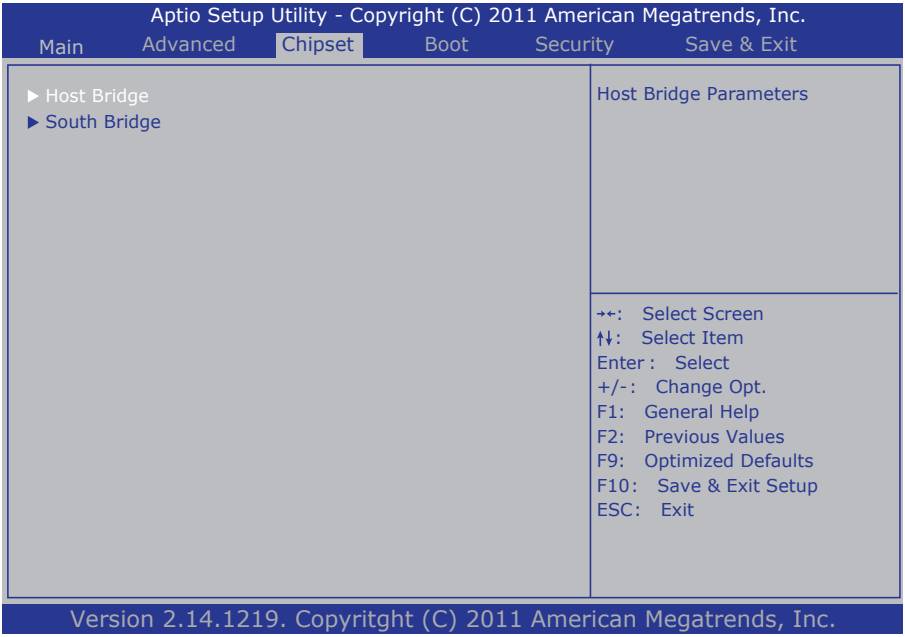
Use the Serial port option to enable or disable the serial port.
The choice: Enabled, Disabled

Change Settings

Use the Change Settings option to change the serial port's IO port address and interrupt address.
The choice:
Auto
IO=3F8h; IRQ=4,
IO=3F8h; IRQ=3,4,5,6,7,10,11,12
IO=2F8h; IRQ=3,4,5,6,7,10,11,12
IO=3E8h; IRQ=3,4,5,6,7,10,11,12
IO=2E8h; IRQ=3,4,5,6,7,10,11,12

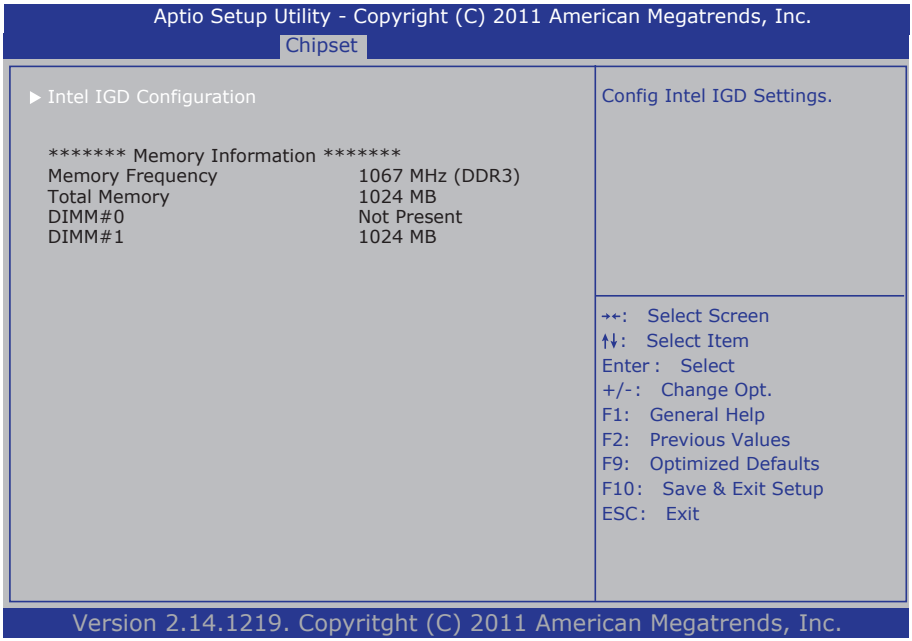
3.3 Chipset

This section allows you to configure and improve your system; also, set up some system features according to your preference.

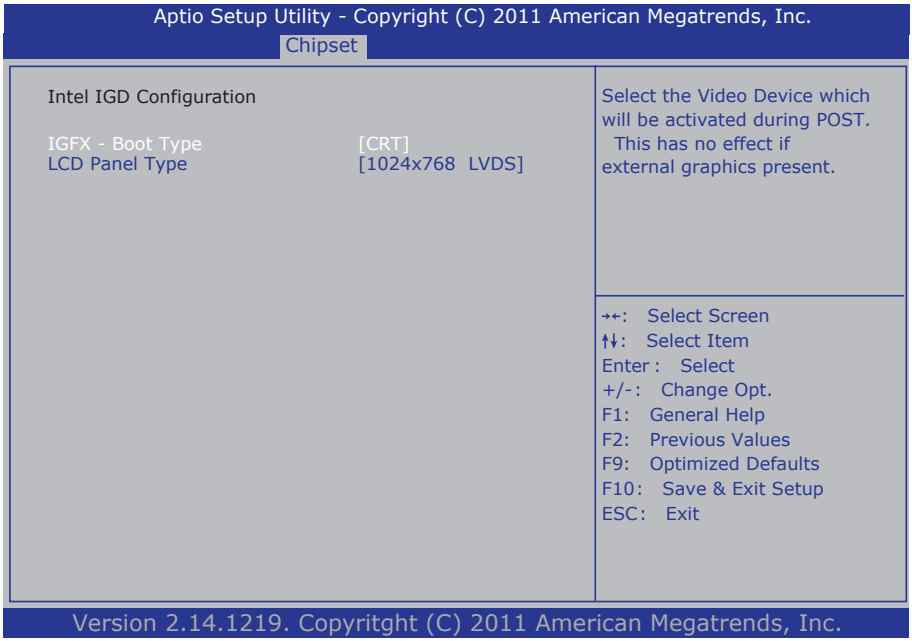


3.3.1 Host Bridge Parameters

Memory Frequency and Timing



Intel IGD Configuration



IFGX - Boot Type

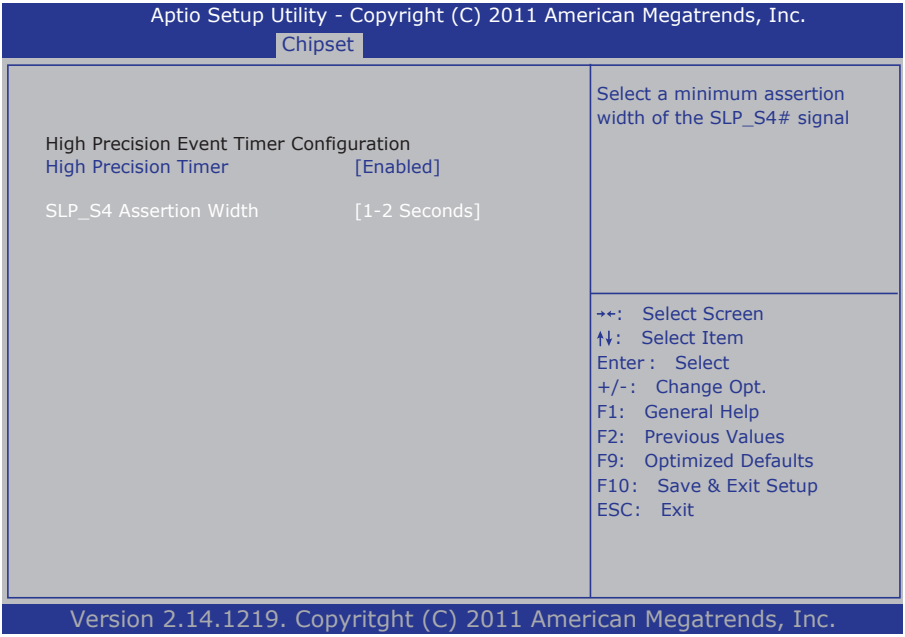
Select the Video Device which will be activated during POST. This has no effect if external graphics present.

LCD Panel Type

Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item:

640x480 LVDS
800x600 LVDS
1024x768 LVDS
1280x1024 LVDS
1366x768 LVDS
1366x768 24bit LVDS
1024x768 24bit LVDS
1024x600 LVDS
1280x600 LVDS.

3.3.2 SB Configuration



High Precision TImer

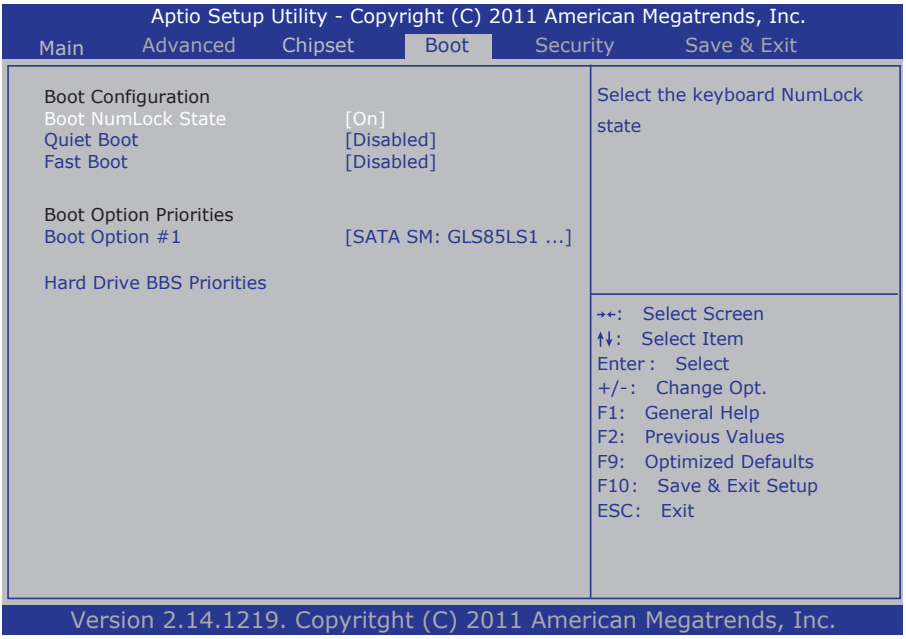
Enables or Disables High Precision Timer.

SLP_S4 Assertion Width

Select a minimum assertion width of the SLP_S4# signal.
The choice: 1-2 Seconds, 2-3 Seconds, 3-4 Seconds, 4-5 Seconds

3.4 Boot Settings

The Boot menu items allow you to change the system boot options.



Boot Configuration

Bootup NumLock State

This setting determines whether the Num Lock key should be activated at boot up.

Quiet Boot

This allows you to select the screen display when the system boots.

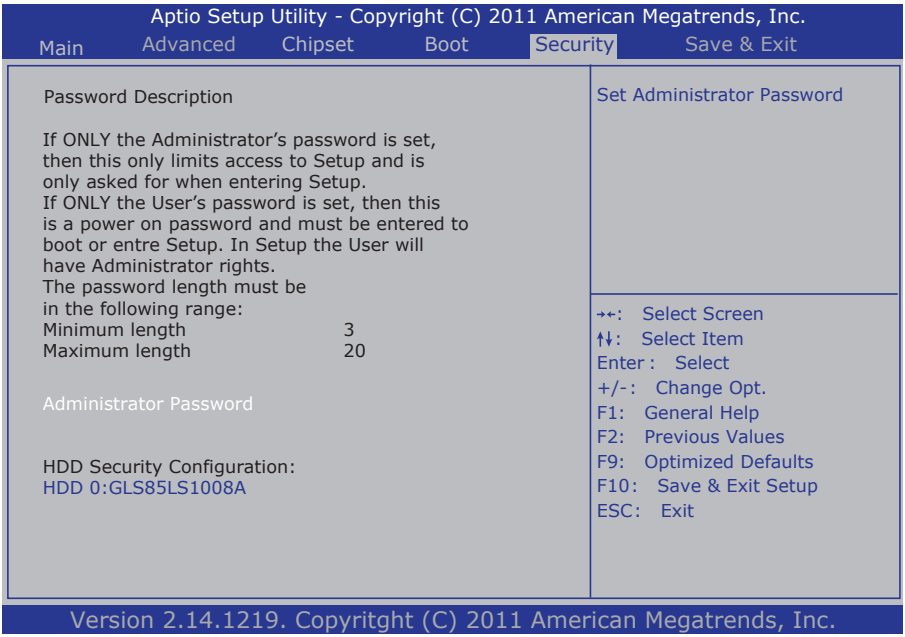
Boot Option Priorities

Select the boot sequence of the hard drives.

Hard Drive BBS Priorities

This allows you to set the hard drive boot priority. The BIOS will attempt to arrange the hard disk boot sequence automatically. You can also change the booting sequence. The number of device items that appears on the screen depends on the number of devices installed in the system.

3.5 Security



Administrator Password

Use the Administrator Password to set or change a administrator password.

ENTER PASSWORD

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <ESC> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED

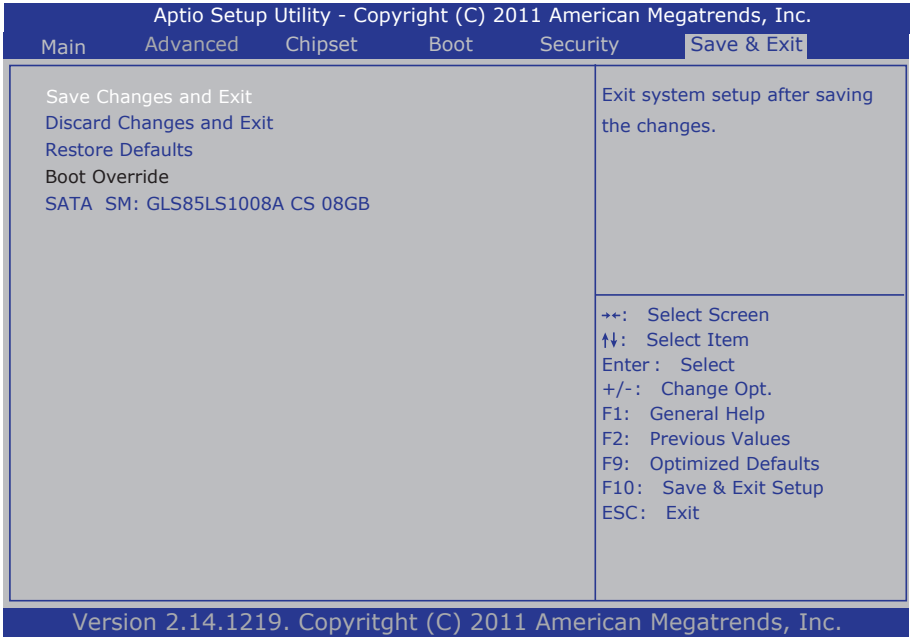
When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from

changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You can determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If it’s set to “Setup”, prompting only occurs when trying to enter Setup.

3.6 Save & Exit



Save Changes and Reset

Pressing <Enter> on this item and it asks for confirmation:

Save configuration changes and exit setup?

Pressing <OK> stores the selection made in the menus in CMOS - a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

Restore Defaults

Restore system to factory default.
Pressing <Enter> on this item and it asks for confirmation prior to executing this command.

Boot Override

This group of functions includes a list of tokens, each of them corresponding to one device within the boot order. Select a drive to immediately boot that device regardless of the current boot order.

3.7 AMI BIOS Checkpoints

3.7.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

3.7.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed

0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.

0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available

0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)

0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable

0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found

0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

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Appendix

Appendix A: I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
0x00000000-0x00000CF7	PCI bus
0x00000000-0x00000CF7	Direct memory access controller
0x00000D00-0x0000FFFF	PCI bus
0x0000F000-0x0000F03F	Video Controller (VGA Compatible)
0x0000F060-0x0000F07F	Ethernet Controller
0x00000A79-0x00000A79	ISAPNP Read Data Port
0x00000279-0x00000279	ISAPNP Read Data Port
0x00000274-0x00000277	ISAPNP Read Data Port
0x00000081-0x00000091	Direct memory access controller
0x00000093-0x0000009F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller

0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x000004D0-0x000004D1	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000070-0x00000070	System CMOS/real time clock
0x00000080-0x00000080	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x00001000-0x0000100F	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x00000400-0x00000453	Motherboard resources
0x00000458-0x0000047F	Motherboard resources
0x00000500-0x0000057F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x00000454-0x00000457	Motherboard resources
0x00000A00-0x00000A1F	Motherboard resources
0x00000290-0x0000029F	Motherboard resources
0x00000060-0x00000060	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard

0x00000064-0x00000064	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00000378-0x0000037F	Printer Port (LPT1)
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000044-0x0000005F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x000000F0-0x000000FF	Numeric data processor
0x0000F130-0x0000F137	Standard Dual Channel PCI IDE Controller
0x0000F120-0x0000F123	Standard Dual Channel PCI IDE Controller
0x0000F110-0x0000F117	Standard Dual Channel PCI IDE Controller
0x0000F100-0x0000F103	Standard Dual Channel PCI IDE Controller
0x0000F0F0-0x0000F0FF	Standard Dual Channel PCI IDE Controller
0x0000F0E0-0x0000F0EF	Standard Dual Channel PCI IDE Controller
0x0000F040-0x0000F05F	SM Bus Controller
0x0000F0D0-0x0000F0D7	Standard Dual Channel PCI IDE Controller
0x0000F0C0-0x0000F0C3	Standard Dual Channel PCI IDE Controller
0x0000F0B0-0x0000F0B7	Standard Dual Channel PCI IDE Controller
0x0000F0A0-0x0000F0A3	Standard Dual Channel PCI IDE Controller
0x0000F090-0x0000F09F	Standard Dual Channel PCI IDE Controller
0x0000F080-0x0000F08F	Standard Dual Channel PCI IDE Controller
0x000003B0-0x000003BB	VgaSave
0x000003C0-0x000003DF	VgaSave

0x000001CE-0x000001CF	VgaSave
0x000002E8-0x000002EF	VgaSave

Appendix B: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 9	Microsoft ACPI-Compliant System
IRQ 16	PCI standard PCI-to-PCI bridge
IRQ 16	Standard Enhanced PCI to USB Host Controller
IRQ 16	PCI standard PCI-to-PCI bridge
IRQ 11	Video Controller (VGA Compatible)
IRQ 11	PCI PCI Simple Communications Controller
IRQ 5	Ethernet Controller
IRQ 5	SM Bus Controller
IRQ 22	Microsoft UAA Bus Driver for High Definition Audio
IRQ 23	Standard Enhanced PCI to USB Host Controller
IRQ 8	System CMOS/real time clock
IRQ 0	System timer
IRQ 1	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
IRQ 12	Microsoft PS/2 Mouse
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 13	Numeric data processor
IRQ 19	Standard Dual Channel PCI IDE Controller
IRQ 19	Standard Dual Channel PCI IDE Controller

Appendix C: BIOS Memory Map

Address	Device Description
0xA0000-0xBFFFF	PCI bus
0xA0000-0xBFFFF	VgaSave
0xD0000-0xD3FFF	PCI bus
0xD4000-0xD7FFF	PCI bus
0xD8000-0xDBFFF	PCI bus
0xDC000-0xDFFFF	PCI bus
0xE0000-0xE3FFF	PCI bus
0xE4000-0xE7FFF	PCI bus
0x7DA00000-0xFEAFFFFF	PCI bus
0x7DA00000-0xFEAFFFFF	Motherboard resources
0xF7800000-0xF7BFFFFF	Video Controller (VGA Compatible)
0xE0000000-0xEFFFFFFF	Video Controller (VGA Compatible)
0xF7C2B000-0xF7C2B00F	PCI Simple Communications Controller
0xF7C00000-0xF7C1FFFF	Ethernet Ethernet Controller
0xF7C28000-0xF7C28FFF	Ethernet Ethernet Controller
0xF7C27000-0xF7C273FF	Standard Enhanced PCI to USB Host Controller
0xF7C20000-0xF7C23FFF	Microsoft UAA Bus Driver for High Definition Audio
0xF7C26000-0xF7C263FF	Standard Enhanced PCI to USB Host Controller
0xFF000000-0xFFFFFFFF	Intel(R) 82802 Firmware Hub Device
0xFF000000-0xFFFFFFFF	Motherboard resources
0xFED00000-0xFED003FF	High Precision Event Timer, HPET
0xF7C25000-0xF7C250FF	SM Bus Controller
0xFED40000-0xFED44FFF	System board
0xFED1C000-0xFED1FFFF	Motherboard resources
0xFED10000-0xFED17FFF	Motherboard resources
0xFED18000-0xFED18FFF	Motherboard resources

0xFED19000-0xFED19FFF	Motherboard resources
0xF8000000-0xFBFFFFFF	Motherboard resources
0xFED20000-0xFED3FFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEEFFFFF	Motherboard resources
0x20000000-0x201FFFFF	System board
0x40000000-0x401FFFFF	System board

Appendix D: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming I/O ports. Below are the source codes written in C, please take them as WDT application example.

```
/*-----  Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define SIO_INDEX       0x2E                /* or index = 0x4E */
#define SIO_DATA        0x2F                /* or data  = 0x4F */

/*-----  routing, sub-routing -----*/
void main()
{
        outportb(SIO_INDEX, 0x87);              /* SIO - Enable */
        outportb(SIO_INDEX, 0x87);

        outportb(SIO_INDEX, 0x07);              /* LDN - WDT */
        outportb(SIO_DATA,  0x07);

        outportb(SIO_INDEX, 0x30);              /* WDT - Enable */
        outportb(SIO_DATA,  0x01);

        outportb(SIO_INDEX, 0xF6);              /* WDT - Timeout Value : 5sec */
        outportb(SIO_DATA,  0x05);

        outportb(SIO_INDEX, 0xFA);              /* WDOUT - Enable */
        outportb(SIO_DATA,  0x01);

        outportb(SIO_INDEX, 0xF5);              /* WDT - Configuration */
        outportb(SIO_DATA,  0x31);

        outportb(SIO_INDEX, 0xAA);              /* SIO - Disable */
}
```

Appendix E: Digital I/O Setting

Below are the source codes written in C, please take them for Digital I/O application examples. The default I/O address is 4Eh/4Fh.

C language Code

```
#define SIO_ID              0x1010

#define SIO_INDEX  0x4E
#define SIO_DATA            0x4F
#define SIO_EN              0x87
#define SIO_DN              0xAA

#define LDN_ADDR   0x07

bool __fastcall TForm1::Check_ID(void)
{
    DWORD iData;

    SetPortVal(SIO_INDEX,SIO_EN,1);// SIO - Enable
    SetPortVal(SIO_INDEX,SIO_EN,1);

    SetPortVal(SIO_INDEX,SIO_EN,1);
    SetPortVal(SIO_INDEX,0x01,1);
    SetPortVal(SIO_INDEX,0x55,1);
    SetPortVal(SIO_INDEX,0x55,1);

    SetPortVal(SIO_INDEX,LDN_ADDR,1);       // LDN - Configure Control
    SetPortVal(SIO_DATA,0x04,1);

    SetPortVal(SIO_INDEX,0x20,1);                   // ID Address
    GetPortVal(SIO_DATA,&iData,1);
    iID = iData;
    SetPortVal(SIO_INDEX,0x21,1);
    GetPortVal(SIO_DATA,&iData,1);
    iID = ( iID << 8 ) + iData;

    Label18->Caption = "ID : " + IntToHex((int)iID,3);

    SetPortVal(SIO_INDEX,SIO_DN,1);         // SIO - Disable

    if( iID == SIO_ID ) return true;

    return false;
}
//---------------------------------------------------------------------------

unsigned char __fastcall TForm1::GPIO_Set(unsigned oMode,unsigned char oData)
{
    DWORD iData;

    // SIO - Enable
    SetPortVal(SIO_INDEX,SIO_EN,1);
    SetPortVal(SIO_INDEX,SIO_EN,1);
```

```
    // LDN - GPIO
    SetPortVal(SIO_INDEX,LDN_ADDR,1);
    SetPortVal(SIO_DATA,0x06,1);

    // GPIO5 - Mode
    SetPortVal(SIO_INDEX,0xA0,1);
    SetPortVal(SIO_DATA,oMode,1);

    // GPIO5 - Data
    SetPortVal(SIO_INDEX,0xA1,1);
    SetPortVal(SIO_DATA,oData,1);

    // GPIO5 - Status
    SetPortVal(SIO_INDEX,0xA2,1);
    GetPortVal(SIO_DATA,&iData,1);

    // SIO - Disable
    SetPortVal(SIO_INDEX,SIO_DN,1);

    return iData;
}
//---------------------------------------------------------------------------

bool __fastcall TForm1::DIO_Test(int iPIN)
{
    int i = iPIN;
        bool bTest = true;
        unsigned char InData;
        unsigned char oMode[8]  = {0x0F,0x0F,0x0F,0x0F,0xF0,0xF0,0xF0,0xF0};
        unsigned char oDataL[8] = {0xF7,0xFD,0xFE,0xFB,0xEF,0xDF,0xBF,0x7F};
        unsigned char oDataH[8] = {0xF8,0xF2,0xF1,0xF4,0x1F,0x2F,0x4F,0x8F};
        unsigned char iData[8]  = {0x10,0x20,0x40,0x80,0x08,0x02,0x01,0x04};


        InData = GPIO_Set(oMode[i],oDataL[i]) & iData[i];    // Low Test
        if( !(InData == 0x00) )    bTest = false;

        InData = GPIO_Set(oMode[i],oDataH[i]) & iData[i];    // Hi Test
        if( !InData )                                bTest = false;

    return bTest;
}
//---------------------------------------------------------------------------
```

Digital IO usage table (Super IO chipaset Fintek F81866D)

Pin	Description	Chipset Pin#	Chipset Pin description
1	DIO1	9	GPIO50
2	DIO2	10	GPIO51
3	DIO3	11	GPIO52
4	DIO4	12	GPIO53
5	DIO5	13	GPIO54
6	DIO6	14	GPIO55
7	DIO7	15	GPIO56
8	DIO8	16	GPIO57