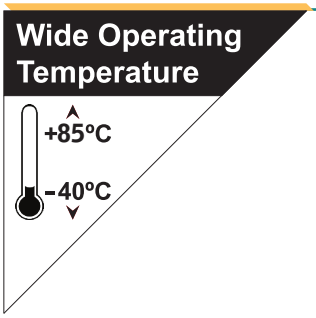


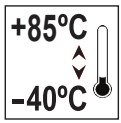
COM-873E

Wide Range Temperature
COM Express Type 2 CPU Module

User's Manual

Version 1.0

2012.06



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Contents

Chapter 1

Introduction

1.1 Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

1.2 Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

> Warning
>
> This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

1.3 About This User's Manual

This user's manual provides general information and installation instructions about the product. This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. please consult your vendor before further handling.

1.4 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

1.5 Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

1.6 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw

E-mail:info@arbor.com.tw

1.7 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

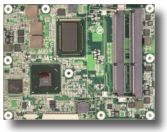
Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.8 Packing List

Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:



1 x COM-873E COM Express CPU Module

1 x Driver CD

1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

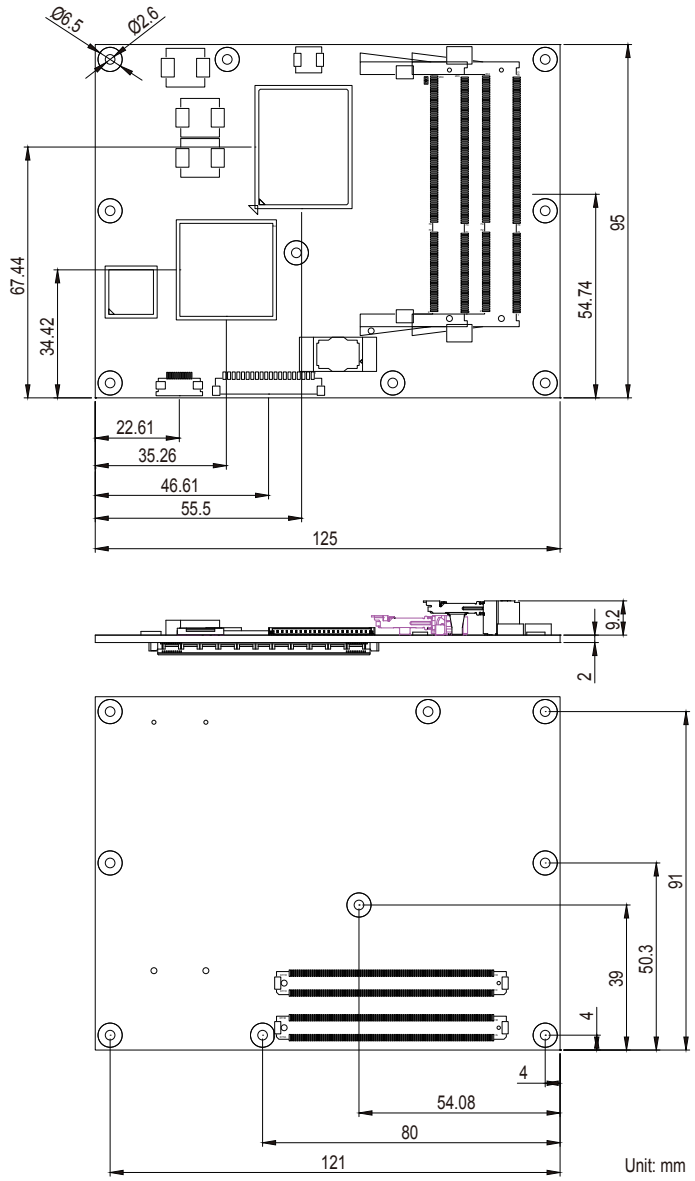
1.9 Ordering Information

COM-873E-2610UE	Soldered onboard Intel Core i7-2610UE/ PCH QM67 COM express WT CPU module
COM-873E-827E	Soldered onboard Intel Celeron 827E / PCH HM65 COM express WT CPU module
FCDB-1424	DisplayPort daughter board
HS-67M1-C1	Wave type heatsink with fan (125x95x34.9mm)
HS-67M1-F1	Heat Spreader (95x125x18mm)
PBE-1700-W R1.3	COM Express Type 2 evaluation board with Winbond W83627 SuperIO in ATX form factor
CBK-04-1700-00	Cable kit 1 x SATA cable 1 x COM port cable 1 x FDD cable 1 x IDE cable

1.10 Specifications

Form Factor	COM Express Type 2 CPU Module
CPU	Soldered onboard Intel® Core i7-2610UE 1.5GHz or Celeron 827E 1.4GHz Processor
Chipset	Intel® PCH QM67 for COM-873E-2610UE Intel® PCH HM65 for COM-873E-827E
System Memory	2 x DDR3 SO-DIMM Socket, supporting 1066/1333MHz SDRAM up to 8GB
Graphics	Integrated Intel® HD Graphics 3000
Display	Analog RGB supports up to 2048 x 1536 @60Hz LCD: Dual channels 24-bit LVDS, up to 1920 x1600 Support DisplayPort Support dual independent displays
Ethernet controller	1 x Intel® 82583V PCIe Gigabit Ethernet controller
BIOS	AMI PnP Flash BIOS
Storage	2 x Serial ATA ports w/ 600MB/s HDD transfer rate 2 x Serial ATA ports w/ 300MB/s HDD transfer rate 1 x Ultra ATA port, supports 2 IDE ports
Digital I/O	8-bit programmable Digital Input/Output
Universal Serial Bus	8 x USB 2.0 ports
Expansion Interface	1 x PCIe x16 lanes 3 x PCIe x1 lanes 4 x PCI masters LPC (Low Pin Count) interface
Power requirement	+12V, 5VSB
Power Consumption	Max. 2.12A/12V with Celeron 827E
Operating Temp.	-40ºC ~ 85ºC (-40ºF ~ 185ºF)
Operating Humidity	0 ~ 90% (non-condensing)
Watchdog Timer	1~ 255 levels Reset
Dimension (L x W)	125 x 95 mm (4.9” x 3.7”)

1.11 Board Dimensions



Chapter 2

Installation

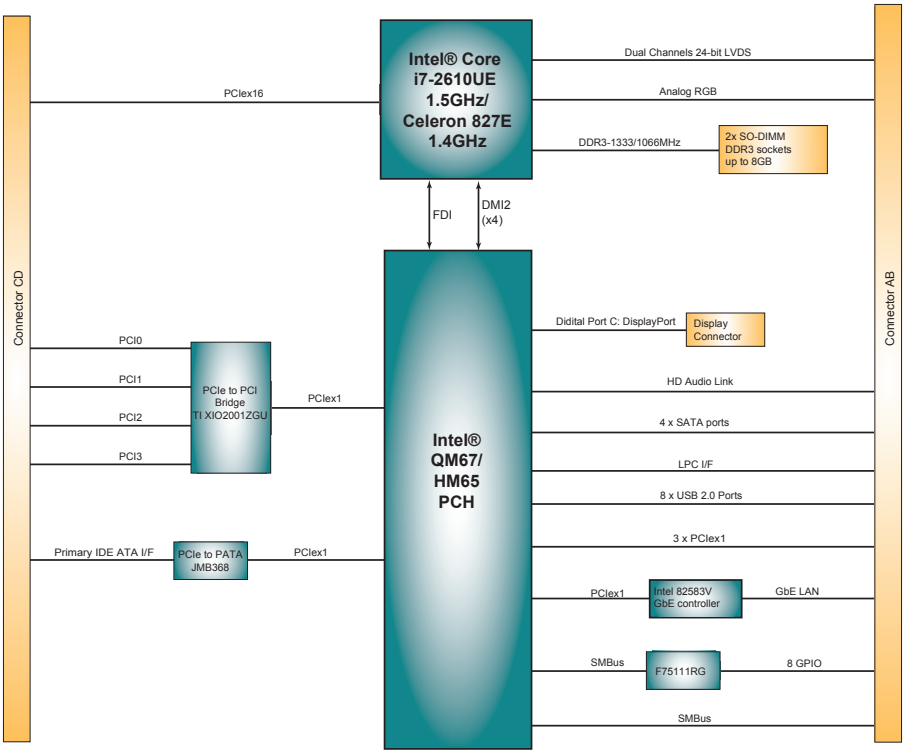
2.1 What is “COM Express”?

With more and more demands on small and embedded industrial boards, a multi-functioned COM (Computer-on-Module) is the great one of the solutions.
COM Express, board-to-board connectors consist of two rows of 220 pins each.
Row AB, which is required, provides pins for PCI Express, SATA, LVDS, LCD channel, LPC bus, system and power management, VGA, LAN, and power and ground interfaces.
Row CD, which is optional, provides SDVO and legacy PCI and IDE signals next to additional PCI Express, LAN and power and ground signals.

By the way, the target markets of COM will be focused on:

- Retail & Advertising
- Medical
- Test & Measurement
- Gaming & Entertainment
- Industrial & Automation
- Military & Government
- Security

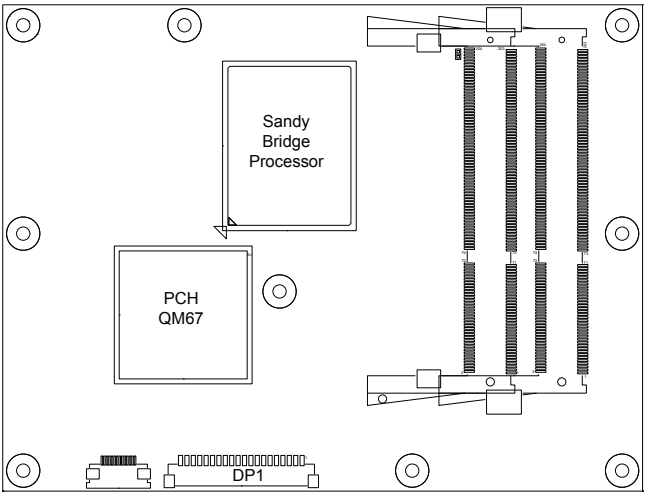
2.2 Block Diagram



2.3 Jumpers and Connectors

Top side

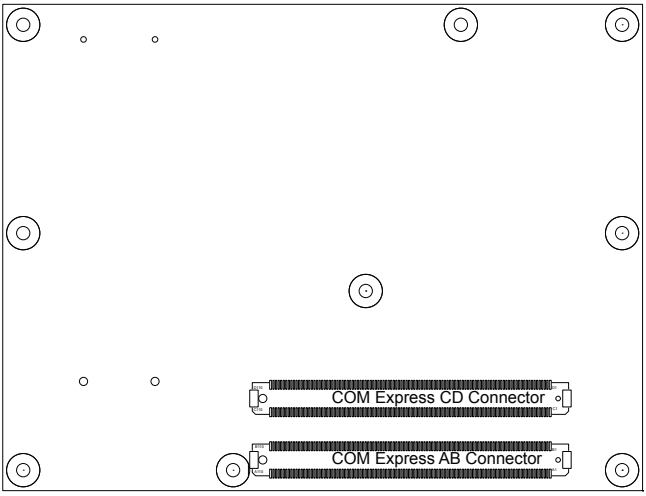
DP1 DisplayPort Connector



Bottom side

COM Express AB Connector

COM Express CD Connector



DP1: DisplayPort connector

Connector type: ACES 1.25mm 88266-200X1

Pin	Desc.	Pin	Desc.
1	LANE_0P	11	LANE_3N
2	LANE_0N	12	GND
3	GND	13	CONF1
4	LANE_1P	14	CONF2
5	LANE_1N	15	AUXP
6	GND	16	AUXN
7	LANE_2P	17	GND
8	LANE_2N	18	HPD
9	GND	19	RTN_PWR
10	LANE_3P	20	PWR(3.3V)

2.4 COM Express AB Connector (bottom side)

B1	GND	GND	A1
B2	GBE0_ACT#	GBE0_MDI3-	A2
B3	LPC_FRAME#	GBE0_MDI3+	A3
B4	LPC_AD0	GBE0_LINK100#	A4
B5	LPC_AD1	GBE0_LINK1000#	A5
B6	LPC_AD2	GBE0_MDI2-	A6
B7	LPC_AD3	GBE0_MDI2+	A7
B8	LPC_DRQ0#	GBE0_LINK#	A8
B9	LPC_DRQ1#	GBE0_MDI1-	A9
B10	LPC_CLK	GBE0_MDI1+	A10
B11	GND	GND	A11
B12	PWRBTN#	GBE0_MDI0-	A12
B13	SMB_CK	GBE0_MDI0+	A13
B14	SMB_DAT	GBE0_CTREF	A14
B15	SMB_ALERT#	SUS_S3#	A15
B16	SATA1_TX+	SATA0_TX+	A16
B17	SATA1_TX-	SATA0_TX-	A17
B18	SUS_STAT#	SUS_S4#	A18
B19	SATA1_RX+	SATA0_RX+	A19
B20	SATA1_RX-	SATA0_RX-	A20
B21	GND	GND	A21
B22	SATA3_TX+	SATA2_TX+	A22
B23	SATA3_TX-	SATA2_TX-	A23
B24	PWR_OK	SUS_S5#	A24
B25	SATA3_RX+	SATA2_RX+	A25
B26	SATA3_RX-	SATA2_RX-	A26
B27	WDT	BATLOW#	A27
B28	AC_SDIN2	ATA_ACT#	A28
B29	AC_SDIN1	AC_SYNC	A29
B30	AC_SDIN0	AC_RST#	A30
B31	GND	GND	A31
B32	SPKR	AC_BITCLK	A32
B33	I2C_CK	AC_SDOUT	A33
B34	I2C_DAT	BIOS_DISABLE#	A34
B35	THRM#	THRMTRIP#	A35
B36	USB7-	USB6-	A36
B37	USB7+	USB6+	A37
B38	USB_4_5_OC#	USB_6_7_OC#	A38
B39	USB5-	USB4-	A39
B40	USB5+	USB4+	A40
B41	GND	GND	A41
B42	USB3-	USB2-	A42
B43	USB3+	USB2+	A43
B44	USB_0_1_OC#	USB_2_3_OC#	A44
B45	USB1-	USB0-	A45
B46	USB1+	USB0+	A46
B47	EXCD1_PERST#	VCC_RTC	A47
B48	EXCD1_CPPE#	EXCD0_PERST#	A48
B49	SYS_RESET#	EXCD0_CPPE#	A49
B50	CB_RESET#	LPC_SERIRQ	A50
B51	GND	GND	A51
B52	PCIE_RX5+	PCIE_TX5+	A52
B53	PCIE_RX5-	PCIE_TX5-	A53
B54	GPO1	GPI0	A54
B55	PCIE_RX4+	PCIE_TX4+	A55

B56	PCIE_RX4-	PCIE_TX4-	A56
B57	GND	GND	A57
B58	PCIE_RX3+	PCIE_TX3+	A58
B59	PCIE_RX3-	PCIE_TX3-	A59
B60	GND	GND	A60
B61	PCIE_RX2+	PCIE_TX2+	A61
B62	PCIE_RX2-	PCIE_TX2-	A62
B63	GPO3	GPI1	A63
B64	PCIE_RX1+	PCIE_TX1+	A64
B65	PCIE_RX1-	PCIE_TX1-	A65
B66	WAKE0#	GND	A66
B67	WAKE1#	GPI2	A67
B68	PCIE_RX0+	PCIE_TX0+	A68
B69	PCIE_RX0-	PCIE_TX0-	A69
B70	GND	GND	A70
B71	LVDS_B0+	LVDS_A0+	A71
B72	LVDS_B0-	LVDS_A0-	A72
B73	LVDS_B1+	LVDS_A1+	A73
B74	LVDS_B1-	LVDS_A1-	A74
B75	LVDS_B2+	LVDS_A2+	A75
B76	LVDS_B2-	LVDS_A2-	A76
B77	LVDS_B3+	LVDS_VDD_EN	A77
B78	LVDS_B3-	LVDS_A3+	A78
B79	LVDS_BKLT_EN	LVDS_A3-	A79
B80	GND	GND	A80
B81	LVDS_B_CK+	LVDS_A_CK+	A81
B82	LVDS_B_CK-	LVDS_A_CK-	A82
B83	CKLVDS_BKLT_CTRL	LVDS_I2C_CK	A83
B84	VCC_5V_SBY	LVDS_I2C_DAT	A84
B85	VCC_5V_SBY	GPI3	A85
B86	VCC_5V_SBY	KBD_RST#	A86
B87	VCC_5V_SBY	KBD_A20GATE	A87
B88	RSVD	PCIE0_CK_REF+	A88
B89	VGA_RED	PCIE0_CK_REF-	A89
B90	GND	GND	A90
B91	VGA_GRN	RSVD B91	A91
B92	VGA_BLU	RSVD	A92
B93	VGA_HSYNC	GPO0	A93
B94	VGA_VSYNC	RSVD	A94
B95	VGA_I2C_CK	RSVD	A95
B96	VGA_I2C_DAT	GND	A96
B97	TV_DAC_A	VCC_12V	A97
B98	TV_DAC_B	VCC_12V	A98
B99	TV_DAC_C	VCC_12V	A99
B100	GND	GND	A100
B101	VCC_12V	VCC_12V	A101
B102	VCC_12V	VCC_12V	A102
B103	VCC_12V	VCC_12V	A103
B104	VCC_12V	VCC_12V	A104
B105	VCC_12V	VCC_12V	A105
B106	VCC_12V	VCC_12V	A106
B107	VCC_12V	VCC_12V	A107
B108	VCC_12V	VCC_12V	A108
B109	VCC_12V	VCC_12V	A109
B110	GND	GND	A110

2.5 COM Express CD Connector (bottom side)

D1	GND	GND	C1
D2	IDE_D5	IDE_D7	C2
D3	IDE_D10	IDE_D6	C3
D4	IDE_D11	IDE_D3	C4
D5	IDE_D12	IDE_D15	C5
D6	IDE_D4	IDE_D8	C6
D7	IDE_D0	IDE_D9	C7
D8	IDE_REQ	IDE_D2	C8
D9	IDE_IOW#	IDE_D13	C9
D10	IDE_ACK#	IDE_D1	C10
D11	GND	GND	C11
D12	IDE_IRQ	IDE_D14	C12
D13	IDE_A0	IDE_IORDY	C13
D14	IDE_A1	IDE_IOR#	C14
D15	IDE_A2	PCI_PME#	C15
D16	IDE_CS1#	PCI_GNT2#	C16
D17	IDE_CS3#	PCI_REQ2#	C17
D18	IDE_RESET#	PCI_GNT1#	C18
D19	PCI_GNT3#	PCI_REQ1#	C19
D20	PCI_REQ3#	PCI_GNT0#	C20
D21	GND	GND	C21
D22	PCI_AD1	PCI_REQ0#	C22
D23	PCI_AD3	PCI_RESET#	C23
D24	PCI_AD5	PCI_AD0	C24
D25	PCI_AD7	PCI_AD2	C25
D26	PCI_C/BE0#	PCI_AD4	C26
D27	PCI_AD9	PCI_AD6	C27
D28	PCI_AD11	PCI_AD8	C28
D29	PCI_AD13	PCI_AD10	C29
D30	PCI_AD15	PCI_AD12	C30
D31	GND	GND	C31
D32	PCI_PAR	PCI_AD14	C32
D33	PCI_SERR#	PCI_C/BE1#	C33
D34	PCI_STOP#	PCI_PERR#	C34
D35	PCI_TRDY#	PCI_LOCK#	C35
D36	PCI_FRAME#	PCI_DEVSEL#	C36
D37	PCI_AD16	PCI_IRDY#	C37
D38	PCI_AD18	PCI_C/BE2#	C38
D39	PCI_AD20	PCI_AD17	C39
D40	PCI_AD22	PCI_AD19	C40
D41	GND	GND	C41
D42	PCI_AD24	PCI_AD21	C42
D43	PCI_AD26	PCI_AD23	C43
D44	PCI_AD28	PCI_C/BE3#	C44
D45	PCI_AD30	PCI_AD25	C45
D46	PCI_IRQC#	PCI_AD27	C46
D47	PCI_IRQD#	PCI_AD29	C47
D48	PCI_CLKRUN#	PCI_AD31	C48
D49	PCI_M66EN	PCI_IRQA#	C49
D50	PCI_CLK	PCI_IRQB#	C50
D51	GND	GND (FIXED)	C51
D52	PEG_TX0+	PEG_RX0+	C52
D53	PEG_TX0-	PEG_RX0-	C53
D54	PEG_LANE_RV#	TYPE0#	C54
D55	PEG_TX1+	PEG_RX1+	C55

D56	PEG_TX1-	PEG_RX1-	C56
D57	TYPE2#	TYPE1#	C57
D58	PEG_TX2+	PEG_RX2+	C58
D59	PEG_TX2-	PEG_RX2-	C59
D60	GND	GND	C60
D61	PEG_TX3+	PEG_RX3+	C61
D62	PEG_TX3-	PEG_RX3-	C62
D63	RSVD	RSVD	C63
D64	RSVD	RSVD	C64
D65	PEG_TX4+	PEG_RX4+	C65
D66	PEG_TX4-	PEG_RX4-	C66
D67	GND	RSVD	C67
D68	PEG_TX5+	PEG_RX5+	C68
D69	PEG_TX5-	PEG_RX5-	C69
D70	GND	GND	C70
D71	PEG_TX6+	PEG_RX6+	C71
D72	PEG_TX6-	PEG_RX6-	C72
D73	SDVO_CLK	SDVO_DATA	C73
D74	PEG_TX7+	PEG_RX7+	C74
D75	PEG_TX7-	PEG_RX7-	C75
D76	GND	GND	C76
D77	IDE_CBLID#	RSVD	C77
D78	PEG_TX8+	PEG_RX8+	C78
D79	PEG_TX8-	PEG_RX8-	C79
D80	GND	GND	C80
D81	PEG_TX9+	PEG_RX9+	C81
D82	PEG_TX9-	PEG_RX9-	C82
D83	RSVD	RSVD	C83
D84	GND	GND	C84
D85	PEG_TX10+	PEG_RX10+	C85
D86	PEG_TX10-	PEG_RX10-	C86
D87	GND	GND	C87
D88	PEG_TX11+	PEG_RX11+	C88
D89	PEG_TX11-	PEG_RX11-	C89
D90	GND	GND	C90
D91	PEG_TX12+	PEG_RX12+	C91
D92	PEG_TX12-	PEG_RX12-	C92
D93	GND	GND	C93
D94	PEG_TX13+	PEG_RX13+	C94
D95	PEG_TX13-	PEG_RX13-	C95
D96	GND	GND	C96
D97	PEG_ENABLE#	RSVD	C97
D98	PEG_TX14+	PEG_RX14+	C98
D99	PEG_TX14-	PEG_RX14-	C99
D100	GND	GND	C100
D101	PEG_TX15+	PEG_RX15+	C101
D102	PEG_TX15-	PEG_RX15-	C102
D103	GND	GND	C103
D104	VCC_12V	VCC_12V	C104
D105	VCC_12V	VCC_12V	C105
D106	VCC_12V	VCC_12V	C106
D107	VCC_12V	VCC_12V	C107
D108	VCC_12V	VCC_12V	C108
D109	VCC_12V	VCC_12V	C109
D110	GND	GND	C110

2.6 The Installation Paths of CD Driver

Windows 2000 & XP

Driver	Path
CHIPSET	\CHIPSET\INF 9.2.0.1021
LAN	\ETHERNET\INTEL\82583V\32
NET Framework	\NET Framework
VGA	\GRAPHICS\INTEL_2K_XP_32\5337 \GRAPHICS\INTEL_2K_XP_64\5337
AUDIO	\AUDIO\REALTEK_HD\WIN2K_XP_x86x64_R257
Management Engine	\ME\MEI_allOS_7.1.13.1088
RAID	\RAID\INTEL\32bit_v10.1.0.1008 \RAID\INTEL\64bit_v10.1.0.1008

Windows 7

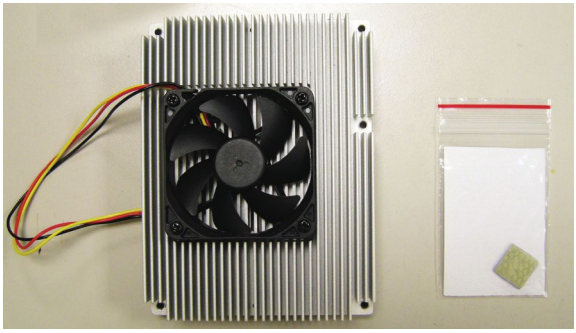
Driver	Path
CHIPSET	\CHIPSET\INF 9.2.0.1021
LAN	\ETHERNET\INTEL\82583V\32 \ETHERNET\INTEL\82583V\64
VGA	\GRAPHICS\INTEL_WIN7_32\2342 \GRAPHICS\INTEL_WIN7_64\2342
AUDIO	\AUDIO\REALTEK_HD\Win7_R257
Management Engine	\ME\MEI_allOS_7.1.13.1088
Intel Turbo	\Intel Turbo

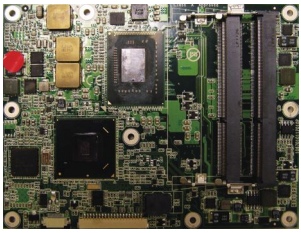
Note: Please install the drivers according to the sequence as below:

CHIPSET → LAN → NET Framework → VGA → AUDIO → Management Engine → RAID / Intel Turbo

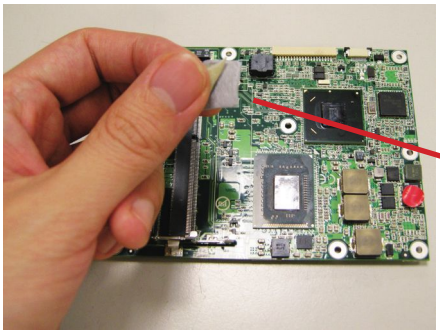
2.7 Heatsink Installation

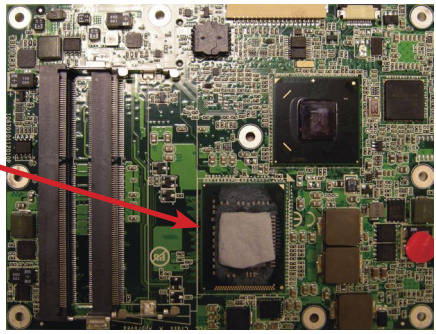
1. Prepare your optional heatsink, thermal pad and CPU module.





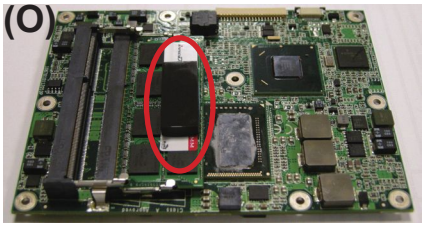
2. For COM-873E-827E, you have to put an additional thermal pad between heatsink and CPU module, but COM-873E-2610UE can skip this step. Please tear protective membranes on both sides from thermal pad first of all, be sure not to pinch or mold the thermal pad, and then put it as right picture.



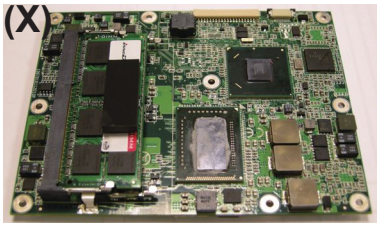


3. You may also apply thermal pad to their memory module. But be aware to put it on the designated place of the first module, as the left illustration, and don't put it on the 2nd module, as right picture, for the 2nd memory module doesn't need it.

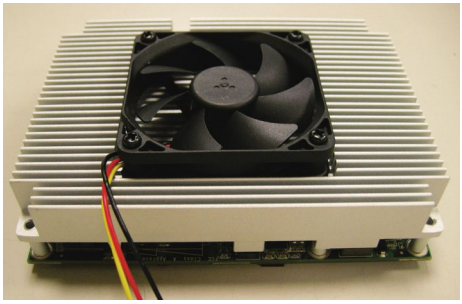
(O)



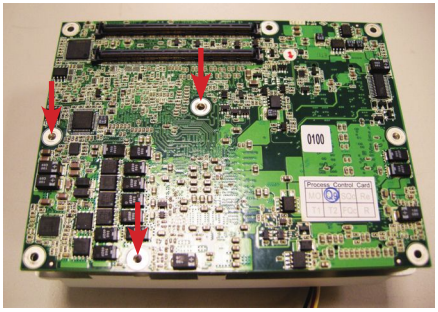
(X)

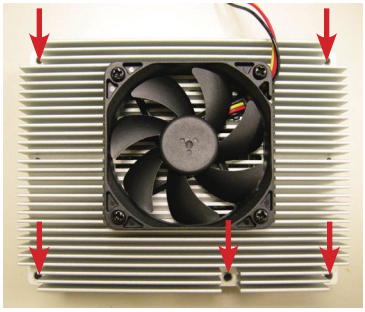


4. After everything is settled down, please assemble heatsink with CPU module according to their corresponding screw positions.



5. Carefully turn them over together and secure the first 3 screws as left picture. Overturn again to secure the rest as right picture.





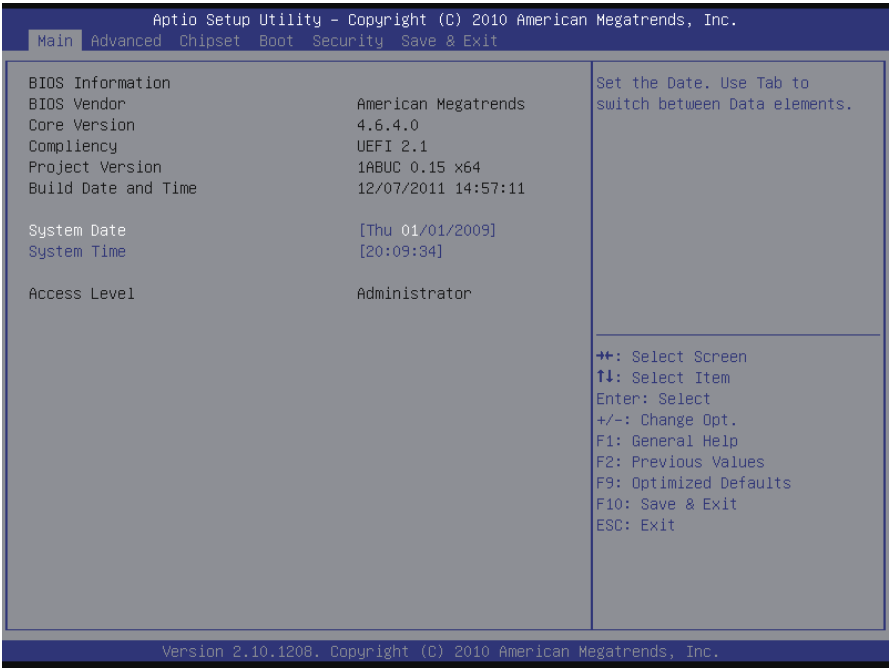
Chapter 3

BIOS

3.1 BIOS Main Setup

The AMI BIOS provides a setup utility program for specifying the system configurations and settings which are stored in the BIOS ROM of the system. When you turn on the computer, the AMI BIOS is immediately activated. After you have entered the setup utility, use the left/right arrow keys to highlight a particular configuration screen from the top menu bar or use the down arrow key to access and configure the information below.

NOTE: In order to increase system stability and performance, our engineering staff are constantly improving the BIOS menu. The BIOS setup screens and descriptions illustrated in this manual are for your reference only, and may not completely match what you see on your screen.



BIOS Information

Display the BIOS information.

System Date

Set the system date. Note that the 'Day' automatically changes when you set the date.

The date format is:

Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1999 to 2099

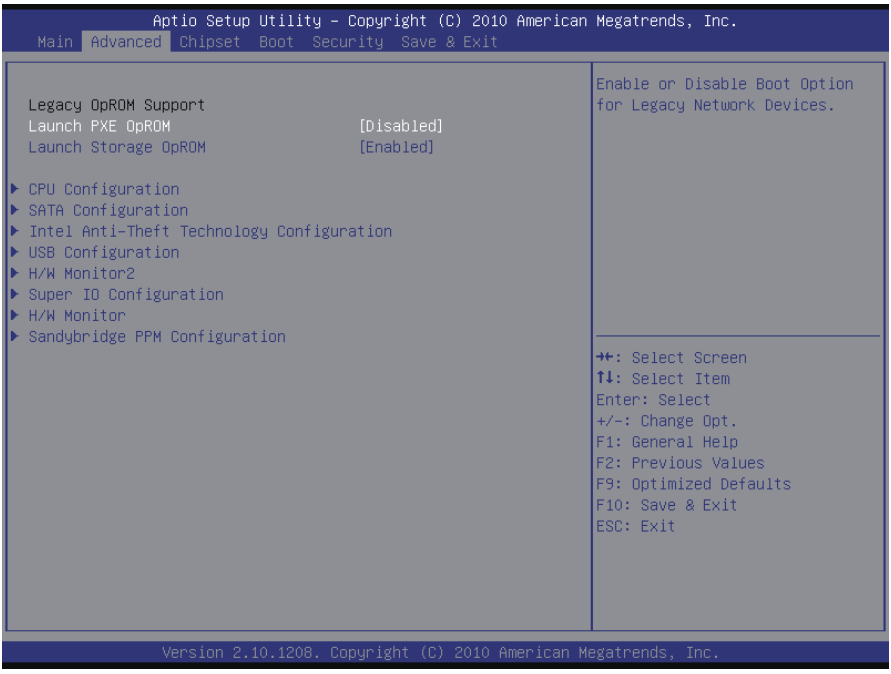
System Time

Set the system time.

The time format is:

Hour : 00 to 23
Minute : 00 to 59
Second : 00 to 59

3.2 Advanced Settings



Legacy OpROM Support

Launch PXE OpROM
Enable or disable the boot option for legacy network devices.

Launch Storage OpROM
Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

CPU Configuration
This section is used to configure the CPU. It will also display detected CPU information.

SATA Configuration
This section is used to configure the SATA drives.

Intel Anti-Theft Technology Configuration
Configure the Intel® Anti-Theft Technology function.

USB Configuration
Configure the USB devices.

H/W Monitor2
This section is used to configure the hardware monitoring events, such as temperature, fan speed and voltages.

Super IO Configuration
This section is used to configure the I/O functions supported by the onboard Super I/O chip.

H/W Monitor
This section is used to configure the hardware monitoring events, such as temperature, fan speed and voltages.

Sandybridge PPM Configuration
Configure periodic permanent magnetic (PPM).

3.2.1 CPU Configuration

The CPU Configuration setup screen varies depending on the installed processor.

Hyper-threading

This item is used to enable or disable the processor's Hyper-threading feature.

Enabled for Windows XP and Linux (OS optimized for Hyper-threading Technology) and disabled for other OS (OS not optimized for Hyper-threading Technology).

When disabled, only one thread per enabled core is enabled.

Limit CPUID Maximum

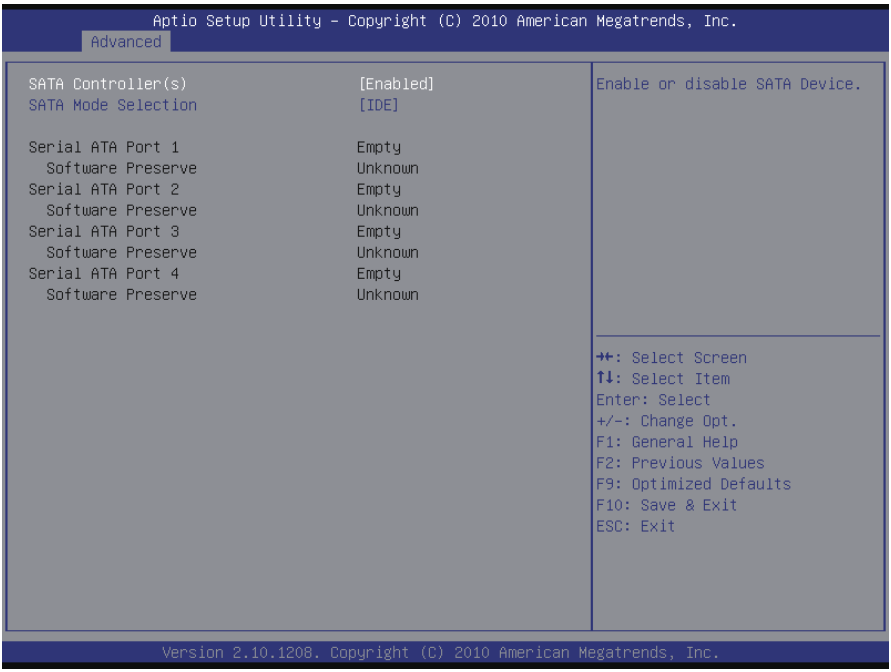
Enable or disable the Limit CPUID Maximum.

Intel Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

3.2.2 SATA Configuration

It allows you to select the operation mode for SATA controller.



SATA Controller(s)

Enable or disable SATA devices.

SATA Mode Selection

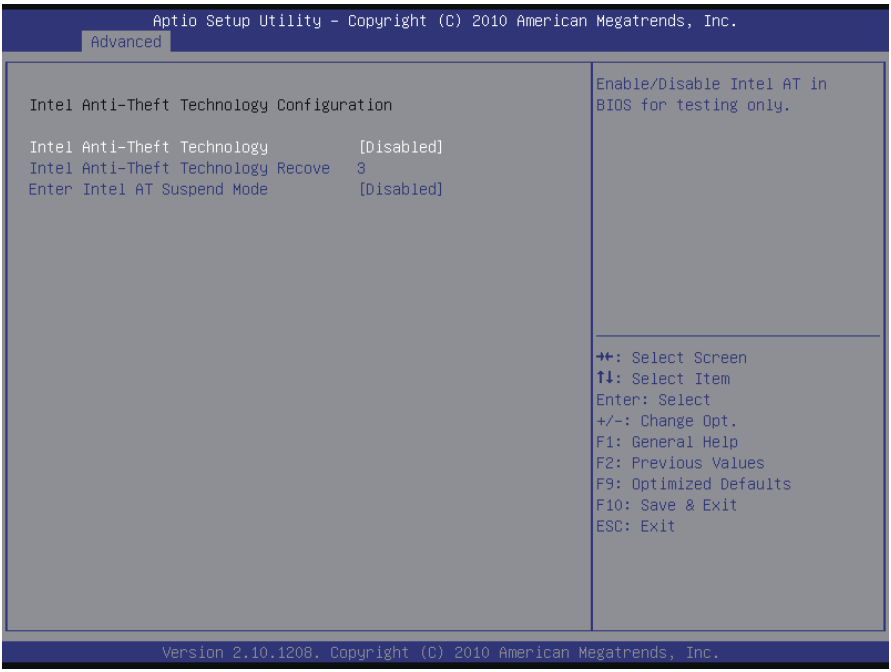
The choice: Disable; IDE (Default), AHCI, RAID

IDE: Set the Serial ATA drives as Parallel ATA storage devices.

AHCI: Allow the Serial ATA devices to use AHCI (Advanced Host Controller Interface).

RAID: Create RAID or Intel Matrix Storage configuration on Serial ATA devices.

3.2.3 Intel Anti-Theft Technology Configuration



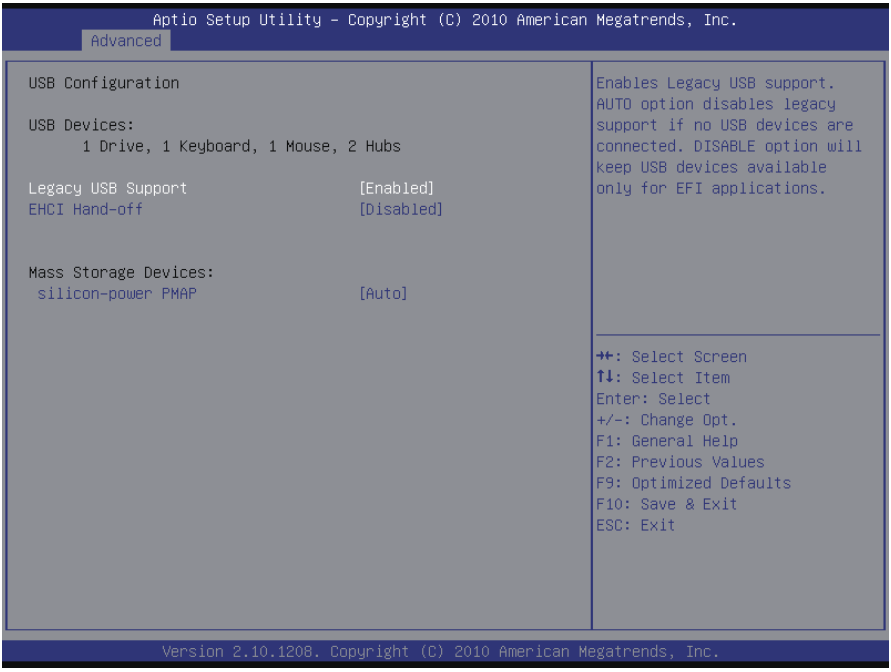
Intel Anti-Theft Technology

Enable or disable Intel® Anti-Theft Technology function in BIOS.

Enter Intel AT Suspend Mode

Enable or disable the request that platform enters AT suspend mode.

3.2.4 USB Configuration



Legacy USB Support

Enable support for legacy USB. AUTO option disables legacy support if no USB devices are connected.
The choice: Enabled (Default); Auto; Disabled

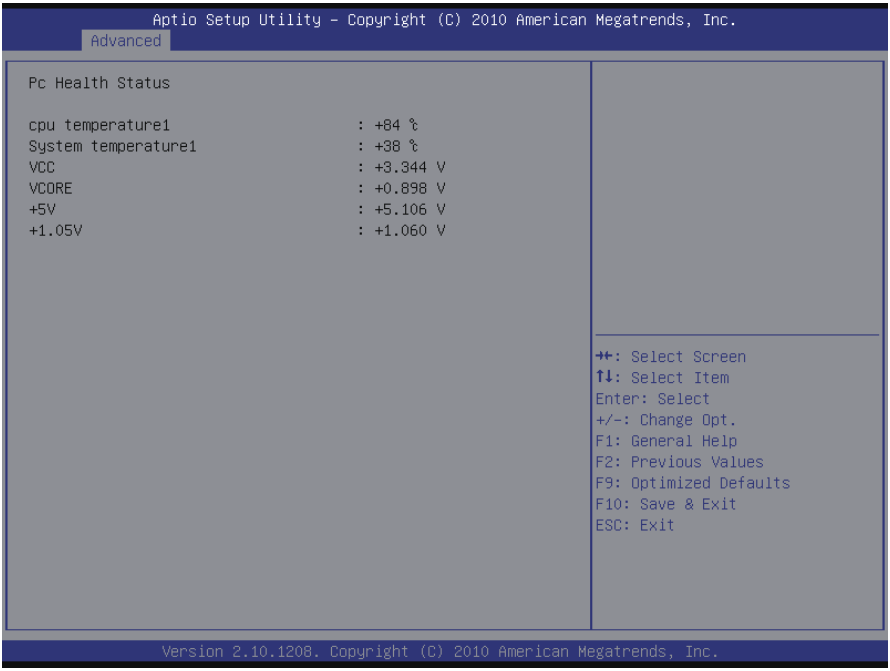
EHCI Hand-off

Allow you to enable support for operating systems without an EHCI hand-off feature. Do not disable the BIOS EHCI Hand-Off option if you are running a Windows® operating system with USB device.
The choice: Enabled (Default); Disabled

Mass Storage Devices

This item displays information when USB devices are detected.

3.2.5 H/W Monitor2

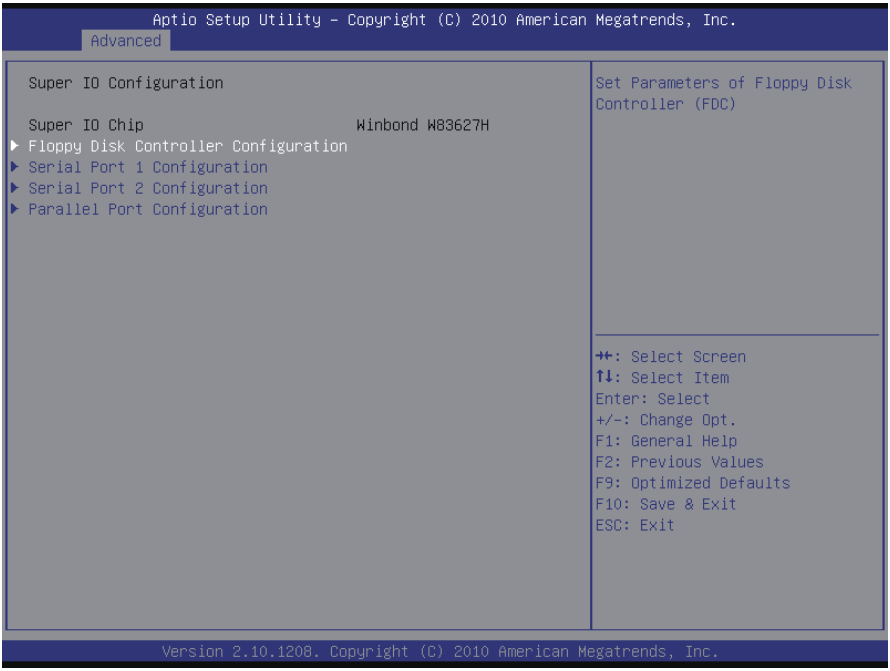


PC Health Status

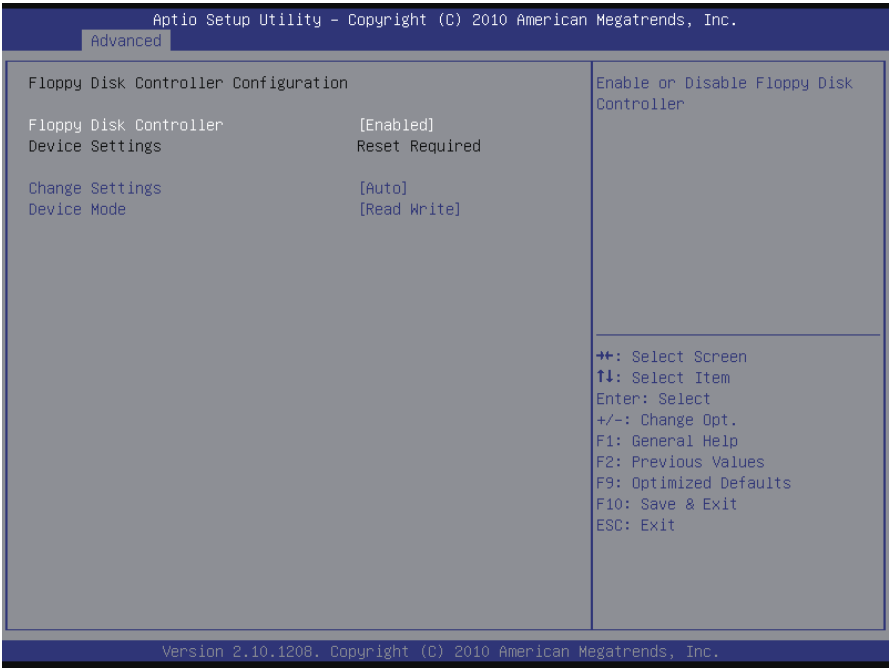
The hardware monitor menu shows the operating temperature and system voltages of CPU module.

3.2.6 Super IO Configuration

You can use this item to set up or change the Super IO configuration for FDD controllers, parallel ports and serial ports.



Floppy Disk Controller Configuration



Floppy Disk Controller

Enable or disable the onboard floppy disk controller.

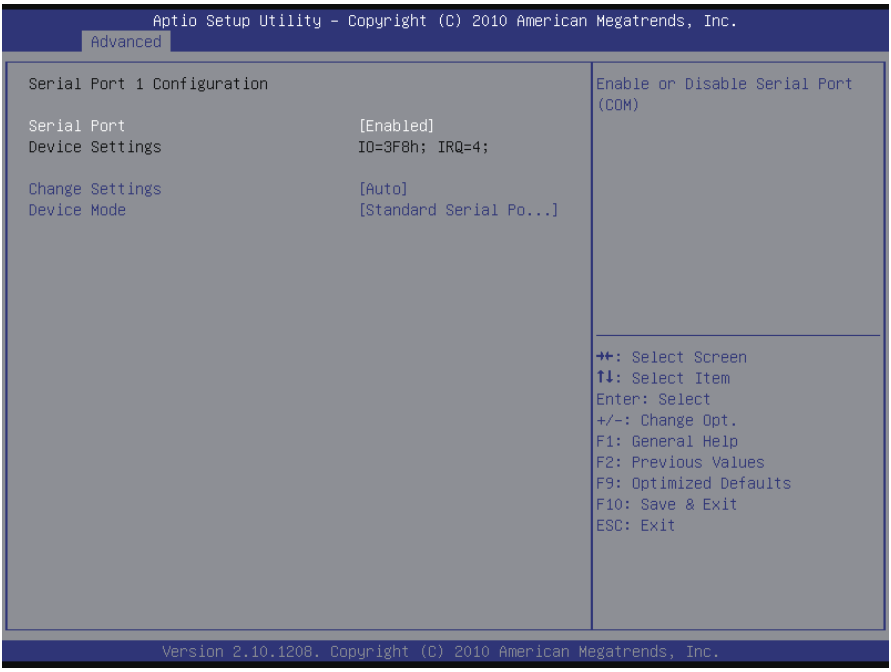
Change Settings

Select the IO/IRQ setting of the I/O device.
The choice: Auto, IO=3F0h; IRQ=6, DMA=2;
IO=3F0h; IRQ=3,4,5,6,7,10,11,12, DMA=2, 3;
IO=370h; IRQ=3,4,5,6,7,10,11,12, DMA=2, 3;

Device Mode

The choice: Read Write, Write Protect

Serial Port 1~2 Configuration



Serial Port

Use the Serial port option to enable or disable the serial port.
The choice: Enabled, Disabled

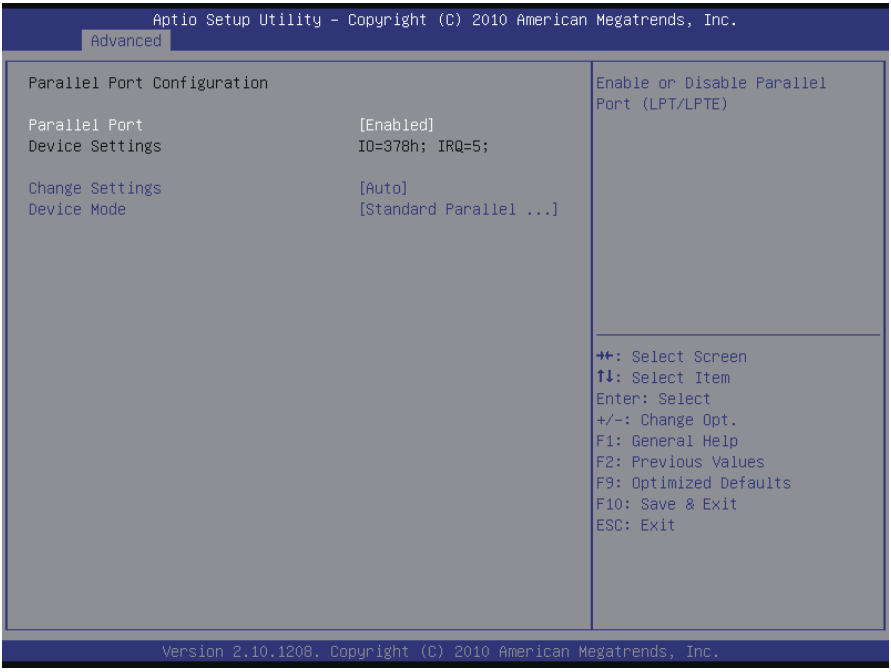
Change Settings

Use the Change Settings option to change the serial port's IO port address and interrupt address.
The choice:
Auto
IO=3F8h; IRQ=4,
IO=3F8h; IRQ=3,4,5,6,7,10,11,12
IO=2F8h; IRQ=3,4,5,6,7,10,11,12
IO=3E8h; IRQ=3,4,5,6,7,10,11,12
IO=2E8h; IRQ=3,4,5,6,7,10,11,12

Device Mode

The choice: Standard Serial Port Mode, IrDA 1.0 (HP SIR) Mode, ASKIR Mode

Parallel Port Configuration



Parallel Port Configuration

This item allows you to enable/disable Parallel Port (LPT/LPTE).

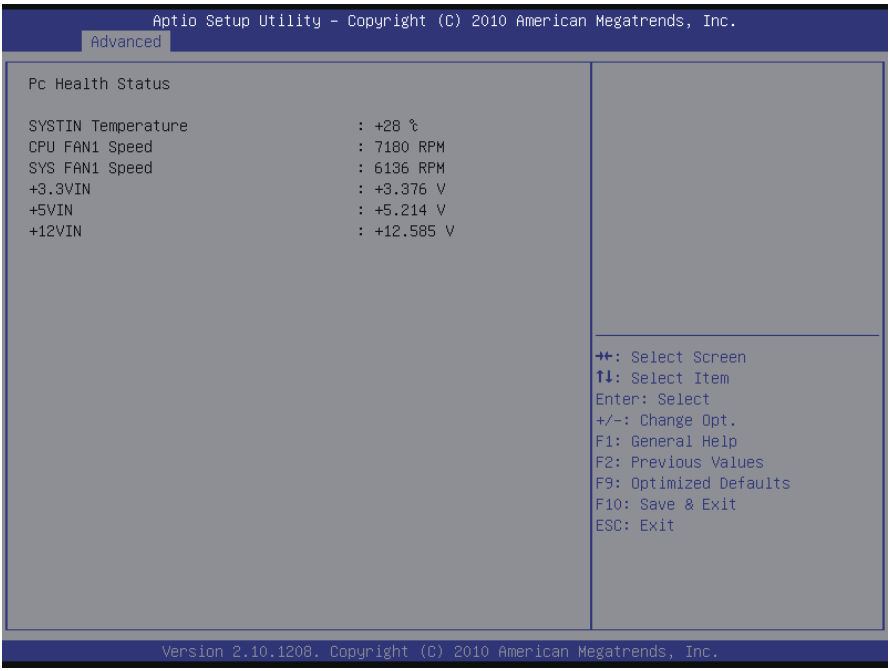
Change Settings

Use the Change Settings option to change the parallel port's IO port address and interrupt address.
The choice:
Auto
IO=378h; IRQ=5,
IO=378h; IRO=5,6,7,10,11,12,
IO=378h; IRQ=5,6,7,10,11,12,
IO=278h; IRQ=5,6,7,10,11,12,
IO=38Ch; IRQ=5,6,7,10,11,12,

Device Mode

The choice: Standard Parallel Port Mode, EPP Mode, ECP Mode, EPP Mode & ECP Mode.

3.2.7 H/W Monitor



PC Health Status

The hardware monitor menu shows the operating temperature, fan speeds and system voltages of PBE-1700.

3.2.8 Sandybridge PPM Configuration

EIST

Enable/Disable Intel SpeedStep.

Turbo Mode

Enable/Disable Turbo Mode.

CPU C3 Report

Enable/Disable CPU C3(ACPI C2) report to OS.

CPU C6 Report

Enable/Disable CPU C6(ACPI C3) report to OS.

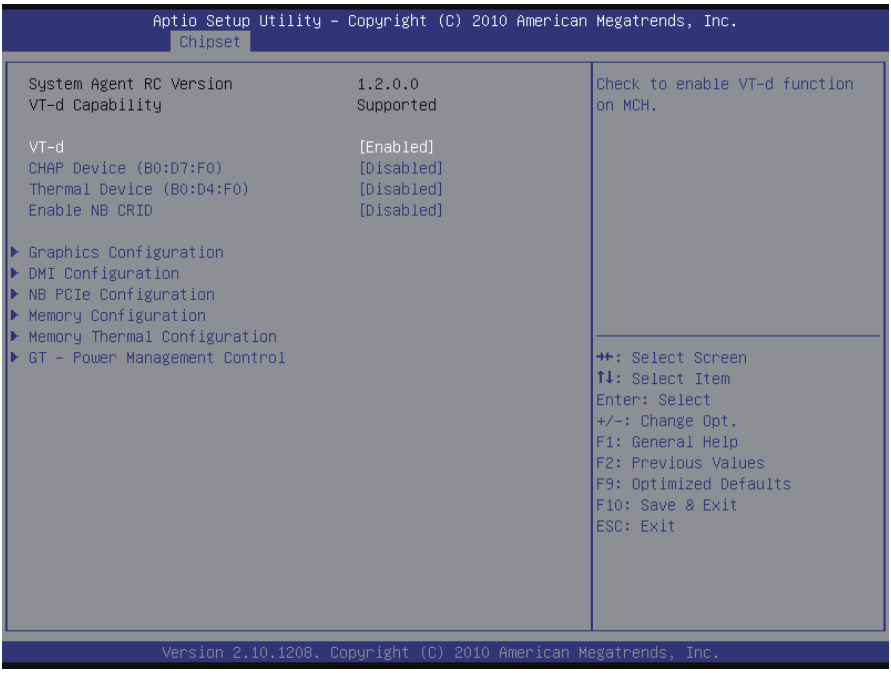
CPU C7 Report

Enable/Disable CPU C7(ACPI C3) report to OS.

3.3 Chipset

This section allows you to configure and improve your system; also, set up some system features according to your preference.

3.3.1 System Agent (SA) Configuration



VT-d

Enable VT-d function on MCH.

CHAP Device (B0:D7:F0)

Enable or disable SA CHAP Device.

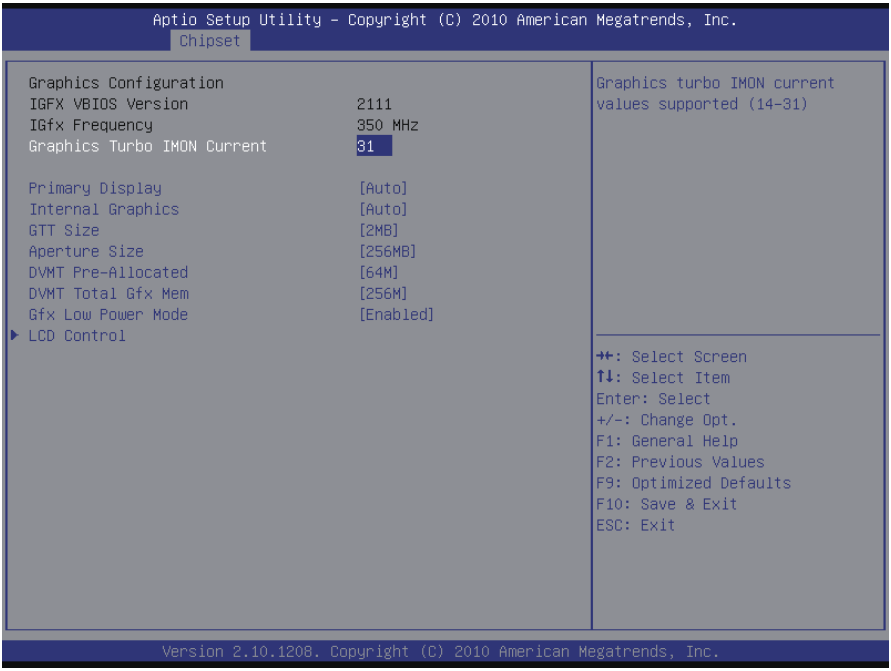
Thermal Device (B0:D4 F0)

Enable or disable SA Thermal Device.

Enable NB CRID

Enable or disable NB CRID WorkAround.

Graphics Configuration



Primary Display

Select which of IGFX/PEG/PCI Graphics Devices should be Primary Display or select SG for Switchable Gfx.

Internal Graphics

Keep IGD enabled based on the option.

GTT Size

Select the GTT Size: 1MB, 2MB.

Aperture Size

Select the Aperture Size: 128MB, 256MB, 512MB.

DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device: 0M~512M.

DVMT Total Gfx Mem

Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device: 128M, 256M, MAX.

Gfx Low Power Mode

This option is applicable for SFF only.

LCD Control

Primary IGFX Boot Display

Select the Video Device which will be activated during POST. This has no effect if external graphics present.
Secondary boot display selection will appear based on your selection.
VGA modes will be supported only on primary display.

LCD Panel Type

Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item: VBIOS Default, 640x480 LVDS ~ 2048x1536 LVDS.

Panel Scaling

Select the LCD panel scaling option used by the Internal Graphics Device: Auto, Off, Force Scaling.

Backlight Control

The choice: PWM Inverted (Default), PWM Normal, GMBus Inverted and GM-Bus Normal.

BIA

The choice: VBIOS Default, Disabled and Level 1/2/3/4/5.

Spread Spectrum clock Chip

The default setting is Off. Other options are:
Hardware: Spread is controlled by chip.
Software: Spread is controlled by BIOS.

Active LFP

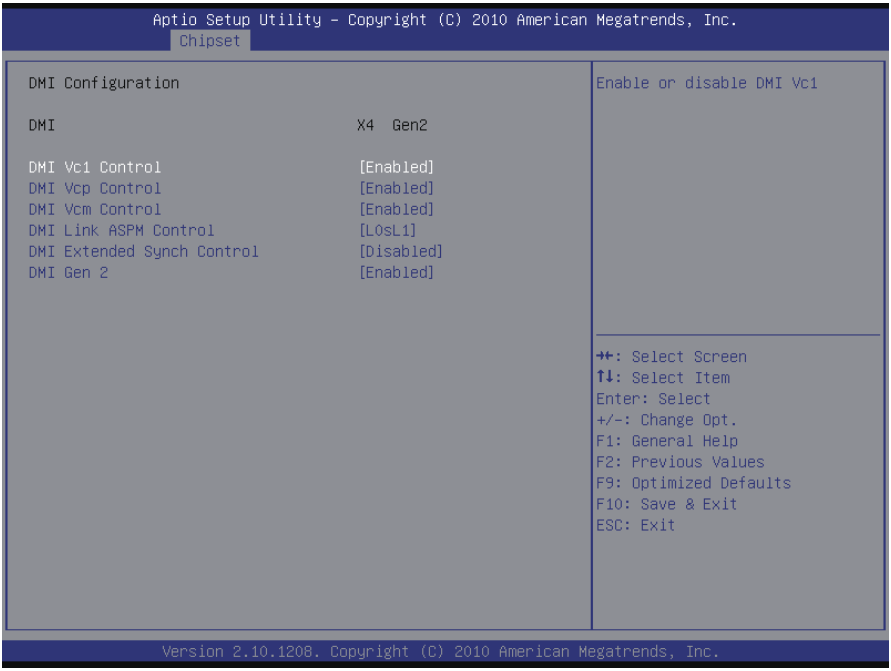
Select the Active LFP Configuration.
No LVDS: VBIOS does not enable LVDS.
Int-LVDS: VBIOS enables LVDS driver by Integrated encoder.
SDVO LVDS: VBIOS enables LVDS driver by SDVO encoder.
eDP Port-A: LFP driven by Int-DisplayPort encoder from Port-A.

Panel Color Depth

Select the LFP panel color depth: 18 Bit, 24 Bit.

DMI Configuration

Control various DMI functions.



DMI Vc1/Vcp/Vcm Control

Enable or disable DMI Vc1/Vcp/Vcm.

DMI Link ASPM Control

Enable or disable the control of Active State Power Management on SA side of the DMI Link.
The choice: Disabled, L0s, L1, L0sL1

DMI Extended Synch Control

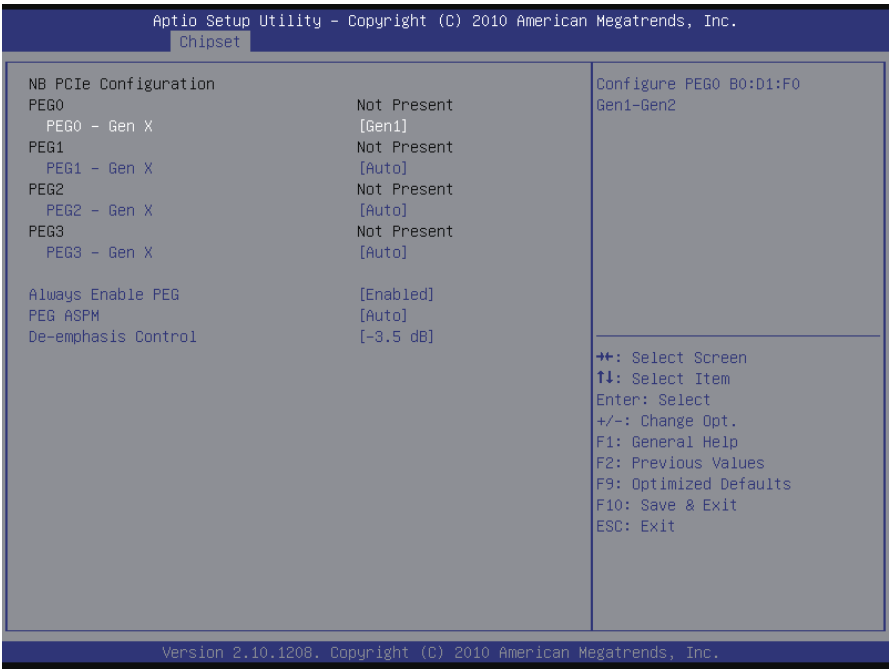
Enable or disable DMI Extended Synchronization.

DMI Gen 2

Enable or disable DMI Gen 2.

NB PCIe Configuration

Configure NB PCIe Express Settings.



PEG0 – Gen X

Configure PEG0 B0:D1:F0 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

PEG1 – Gen X

Configure PEG1 B0:D1:F1 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

PEG2 – Gen X

Configure PEG2 B0:D1:F2 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

PEG3 – Gen X

Configure PEG3 B0:D6:F0 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

Always Enable PEG

Enable the PEG slot.

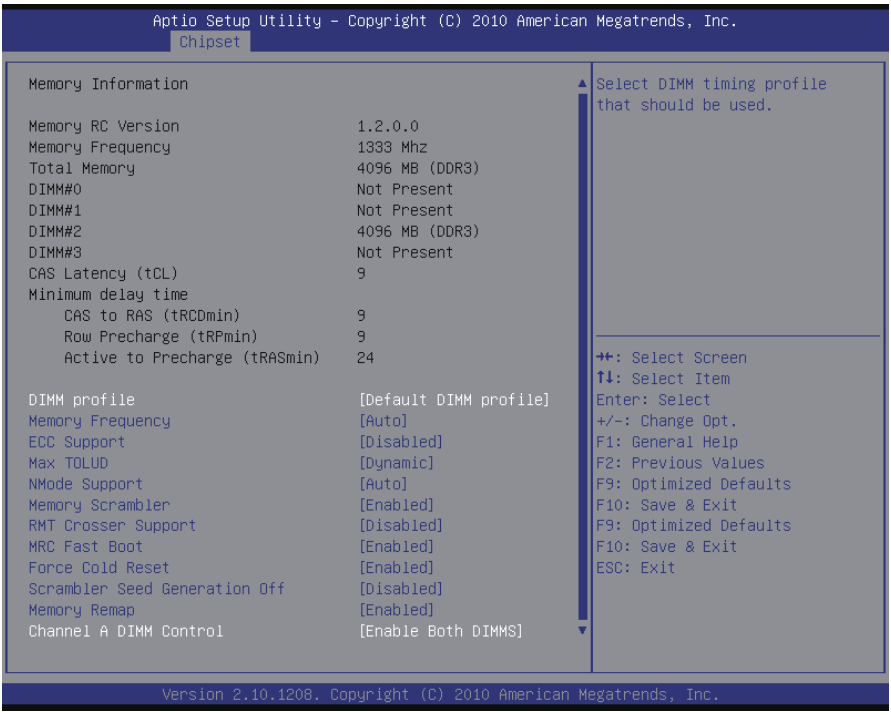
PEG ASPM

Control ASPM support for the PEG Device. This has no effect if PEG is not the currently active device.
The choice: Disabled, Auto, ASPM L0s, ASPM L1, ASPM L0sL1

De-emphasis Control

Configure the De-emphasis control on PEG.
The choice: -6 dB, -3.5 dB

Memory Configuration



DIMM profile

Select DIMM timing profile that should be used.
The choice: Default DIMM profile, XMP profile 1, XMP profile 2

Memory Frequency

Maximum Memory Frequency Selections in Mhz.
The choice: Auto, 1067, 1333, 1600, 1867, 2133

ECC Support

Enable or disable DDR Ecc Support.

Max TOLUD
Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.
The choice: Dynamic, 1GB, 1.25 GB, 1.5 GB, 1.75 GB, 2GB, 2.25 GB, 2.5 GB, 2.75 GB, 3 GB, 3.25 GB

NMode Support
NMode Support Option.
The choice: Auto, 1 N Mode, 2 N Mode

Memory Scrambler
Enable or disable Memory Scrambler support.

RMT Crosser Support
Enable or disable RmtCrosserEnable support.

MRC Fast Boot
Enable or disable MRC fast boot.

Force Cold Reset
Force cold reset or choose MRC cold reset mode, when cold boot is required during MRC execution.
NOTE: If ME 5.0MB is present, Force cold reset is required!

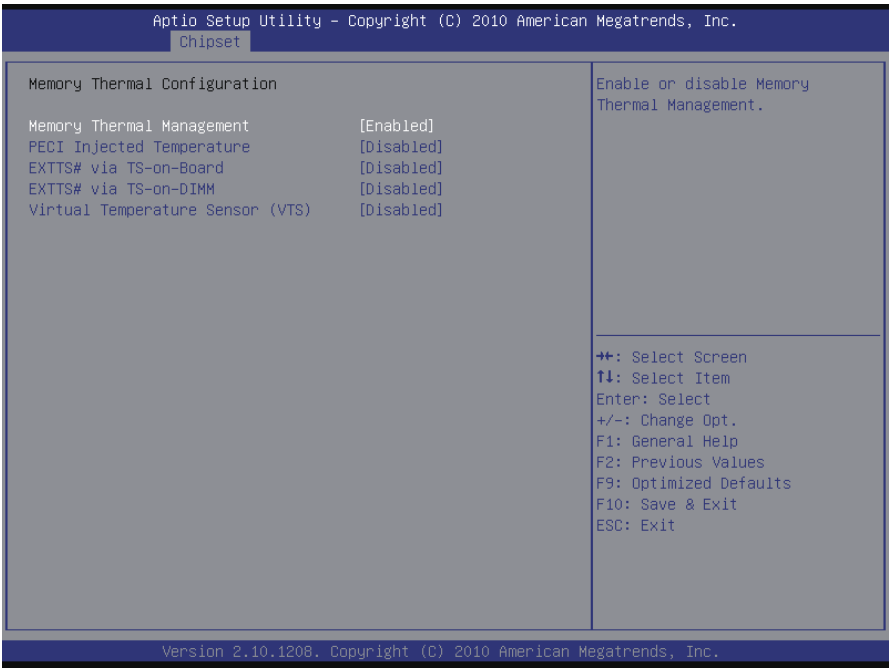
Scrambler Seed Generation Off
Control Memory Scrambler Seed Generation.
Enable - do not generate scrambler seed.
Disable - generate scrambler seed always.

Memory Remap
Enable or disable memory remap above 4G.

Channel A DIMM Control
Enable or disable dimms on channel A.

Memory Thermal Configuration

Memory Thermal Configuration Options.



Memory Thermal Management

Enable or disable Memory Thermal Management.

PECI Injected Temperature

Enable or disable memory temperatures to be injected to the processor via PECI.

EXTT# via TS-on-Board

Enable or disable routing TS-on-Board's ALERT# and THERM# to EXTTS# pins on the PCH.

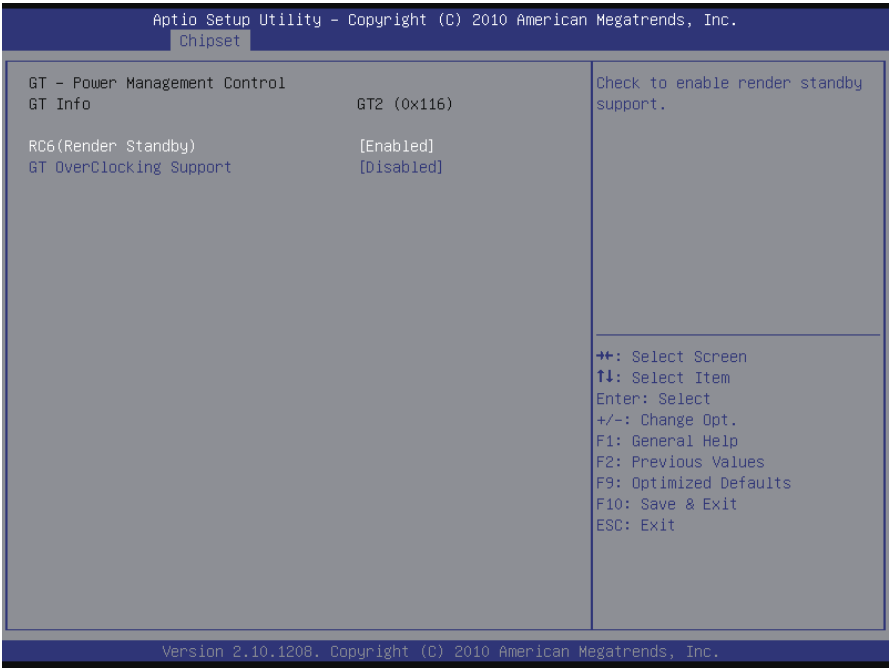
EXTT# via TS-on-DIMM

Enable or disable routing TS-on-DIMM's ALERT# to EXTTS# pin on the PCH.

Virtual Temperature Sensor (VTS)

Enable or disable Virtual Temperature Sensor.

GT – Power Management Control



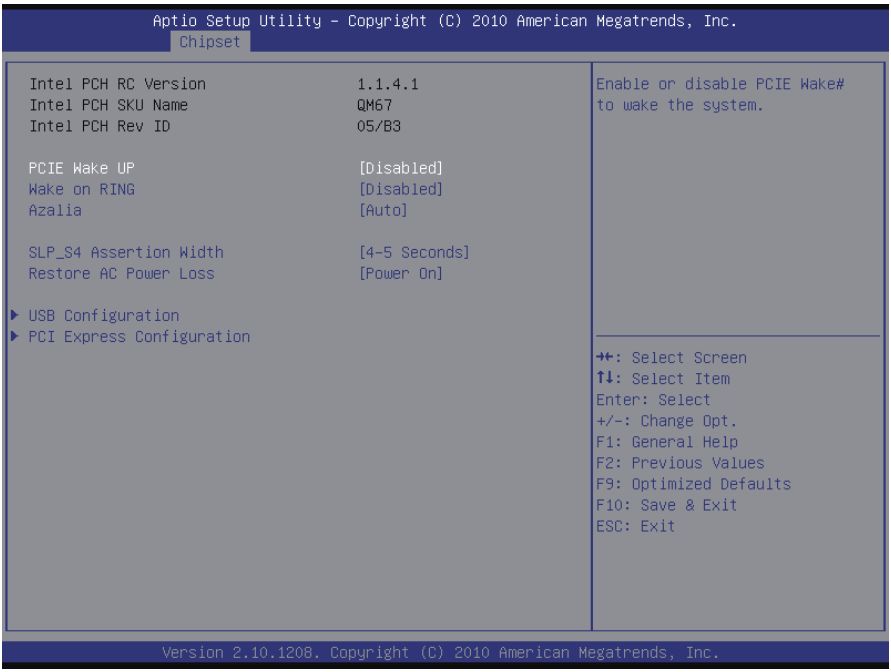
RC6 (Render Standby)

Check to enable render standby support.

GT Overclocking Support

Enable or disable GT Overclocking Support.

3.3.2 PCH-IO Configuration



PCIE Wake UP

Enable or disable PCIE Wake# to wake the system.

Wake on RING

Enable or disable Wake on RING (WOR). Computer will start up simply by applying power to a connected external modem if WOR is enabled.

Azalia

Control detection of the Azalia device.
Disabled = Azalia will be unconditionally disabled.
Enabled = Azalia will be unconditionally enabled.
Auto = Azalia will be enabled if present, disabled otherwise.

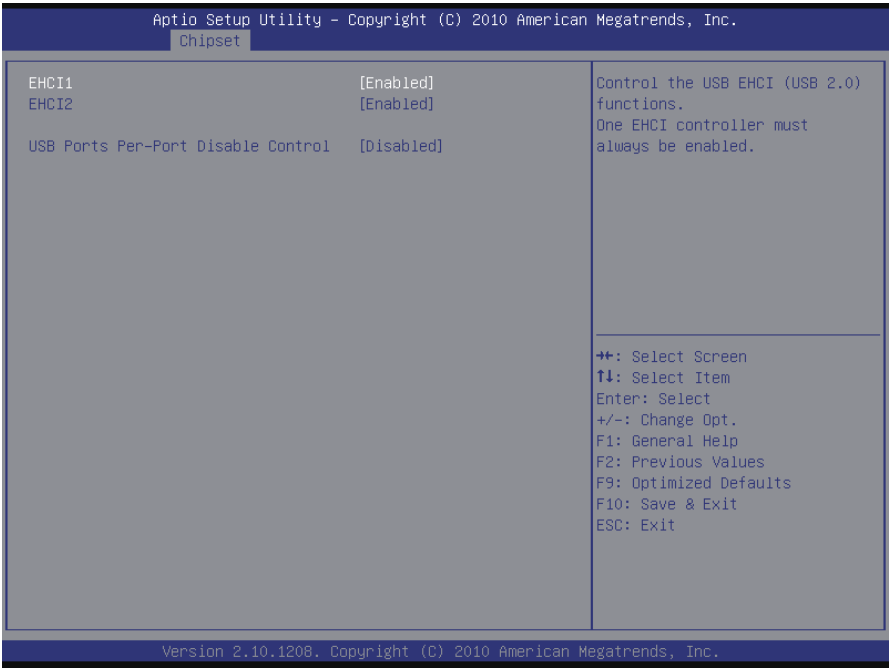
SLP_S4 Assertion Width

Select a minimum assertion width of the SLP_S4# signal.
The choice: 1-2 Seconds, 2-3 Seconds, 3-4 Seconds, 4-5 Seconds

Restore AC Power Loss

Select AC power state when power is re-applied after a power failure.

USB Configuration



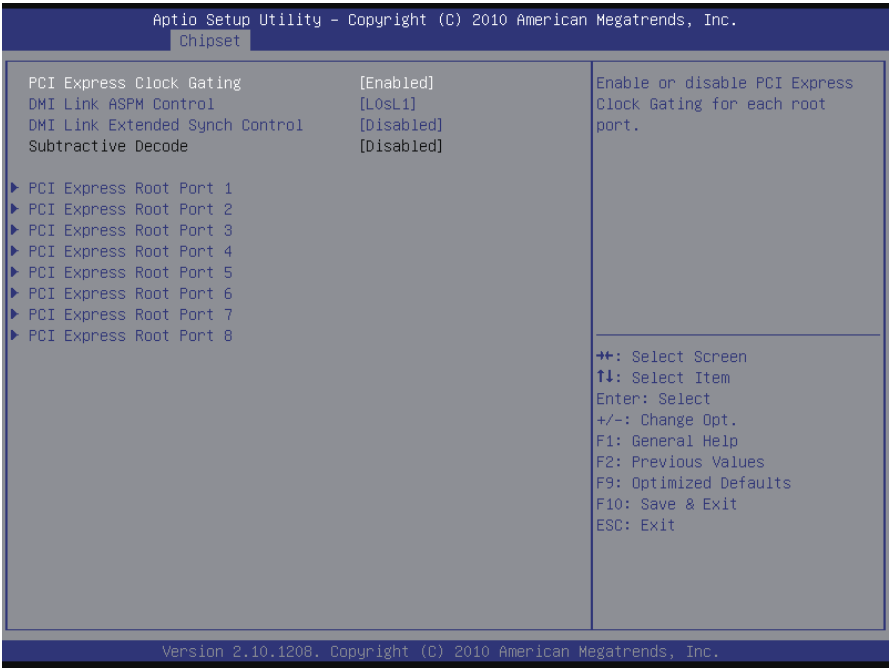
EHCI1~2

Control the USB EHCI (USB2.0) functions.
One EHCI controller must always be enabled.

USB Ports Per-Port Disable Control

Enable or disable each of the USB ports (0~9).

PCI Express Configuration



PCI Express Clock Gating

Enable or disable PCI Express Clock Gating for each root port.

DMI Link ASPM Control

The control of Active State Power Management on both NB side and SB side of the DMI Link.

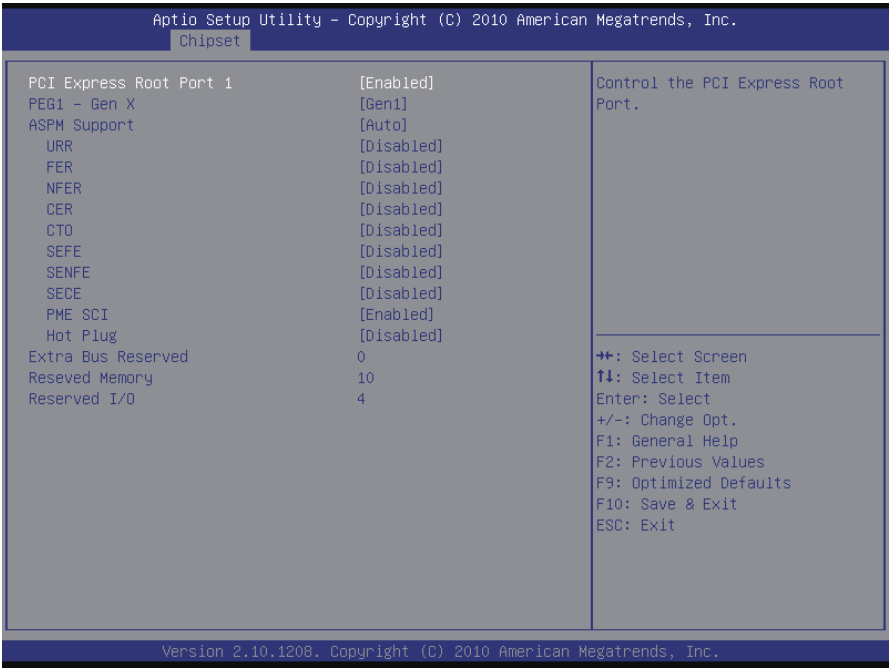
DMI Link Extended Synch Control

The control of Extended Synch on SB side of the DMI Link.

Subtractive Decode

Enable or disable Subtractive Decode.

PCI Express Root Port 1~8



PCI Express Root Port 1~8

Control the PCI Express Root Port.

PEG1 – Gen X

Configure PEG1 B0 :D1 :F1 Gen1-Gen2
The choice: Auto, Gen1, Gen2

ASPM Support

Set the ASPM Level to Disabled, L0s, L1, L0sL1, Auto
Force L0 - Force all links to L0 State
AUTO - BIOS auto configuration
DISABLE - Disable ASPM

URR

Enable or disable PCI Express Unsupported Request Reporting.

FER

Enable or disable PCI Express Device Fatal Error Reporting.

NFER

Enable or disable PCI Express Device Non-Fatal Error Reporting.

CER

Enable or disable PCI Express Device Correctable Error Reporting.

CTO

Enable or disable PCI Express Completion Timer TO.

SEFE

Enable or disable Root PCI Express System Error on Fatal Error.

SENFE

Enable or disable Root PCI Express System Error on Non-Fatal Error.

SECE

Enable or disable Root PCI Express System Error on Correctable Error.

PME SCI

Enable or disable PCI Express PME SCI.

Hot Plug

Enable or disable PCI Express Hot Plug.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

Reserved Memory

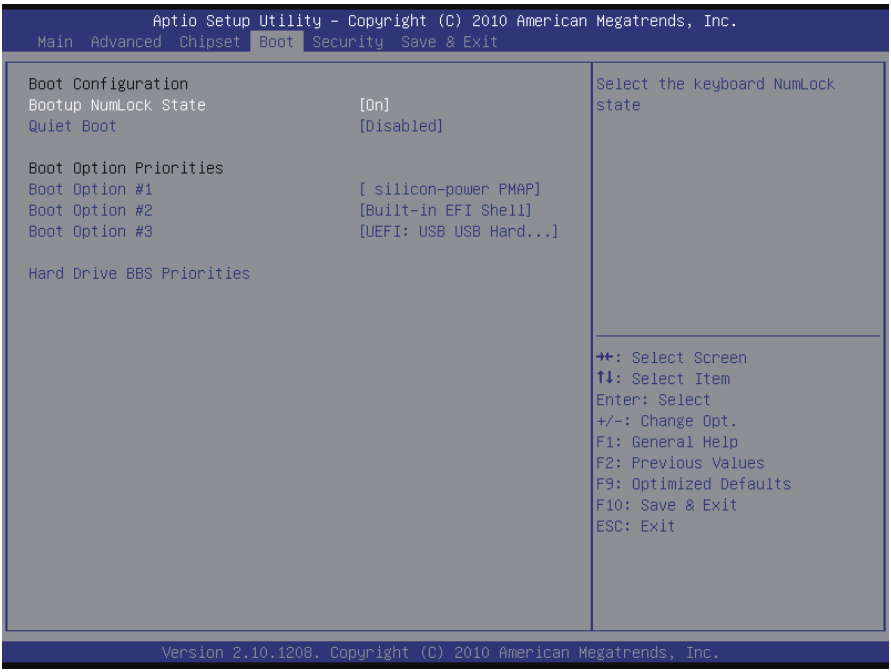
Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserved I/O

Reserved I/O (4k/8k/12k/16k/20k) Range for this Root Bridge.

3.4 Boot Settings

The Boot menu items allow you to change the system boot options.



Boot Configuration

Bootup NumLock State

This setting determines whether the Num Lock key should be activated at boot up.

Quiet Boot

This allows you to select the screen display when the system boots.

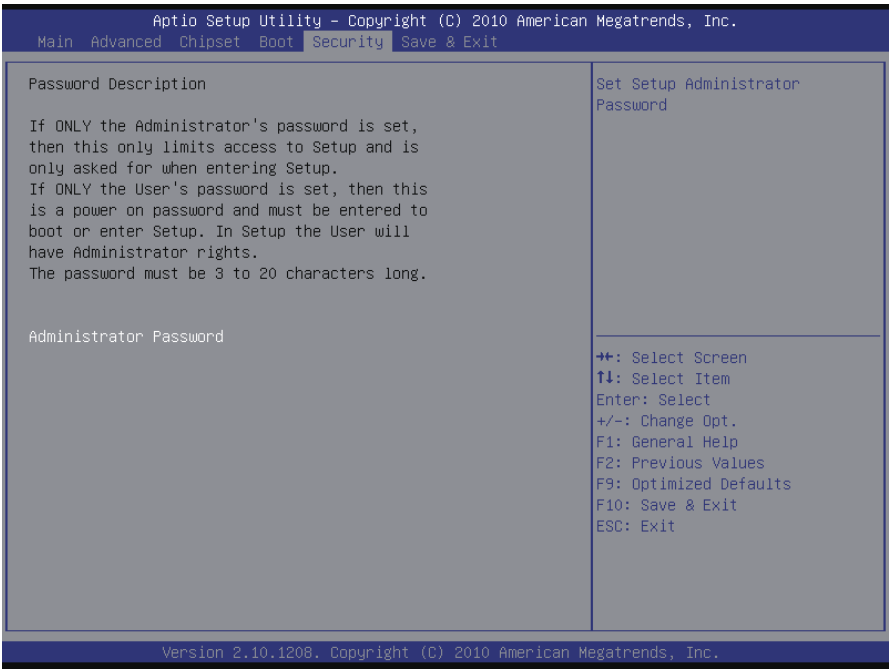
Boot Option Priorities

Select the boot sequence of the hard drives.

Hard Drive BBS Priorities

This allows you to set the hard drive boot priority. The BIOS will attempt to arrange the hard disk boot sequence automatically. You can also change the booting sequence. The number of device items that appears on the screen depends on the number of devices installed in the system.

3.5 Security



Administrator Password

Use the Administrator Password to set or change a administrator password.

ENTER PASSWORD

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <ESC> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED

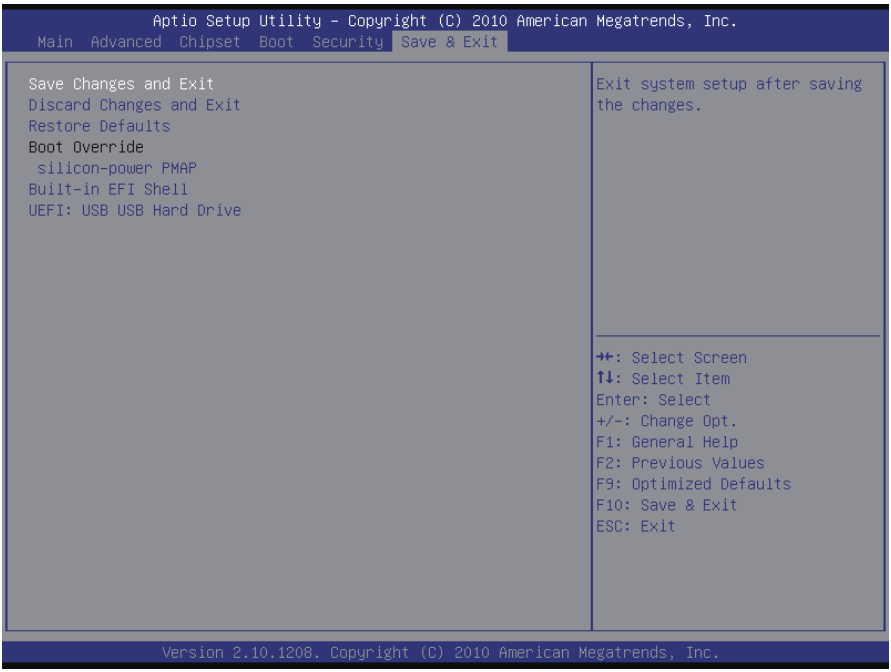
When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from

changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You can determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If it’s set to “Setup”, prompting only occurs when trying to enter Setup.

3.6 Save & Exit



Save Changes and Exit

Pressing <Enter> on this item and it asks for confirmation:

Save configuration changes and exit setup?

Pressing <OK> stores the selection made in the menus in CMOS - a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

Discard Changes and Exit

Exit system setup without saving any changes.
<ESC> key can be used for this operation.

Restore Defaults

Restore system to factory default.
Pressing <Enter> on this item and it asks for confirmation prior to executing this command.

Boot Override

This group of functions includes a list of tokens, each of them corresponding to one device within the boot order. Select a drive to immediately boot that device regardless of the current boot order.

3.7 AMI BIOS Checkpoints

3.7.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

3.7.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed

0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.

0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available

0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)

0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable

0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found

0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

Appendix

Appendix A: I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
00000000-0000001F	Direct memory access controller
00000000-00000CF7	PCI bus
00000010-0000001F	Motherboard resources
00000020-00000021	Programmable interrupt controller
00000022-0000003F	Motherboard resources
00000024-00000025	Programmable interrupt controller
00000028-00000029	Programmable interrupt controller
0000002C-0000002D	Programmable interrupt controller
0000002E-0000002F	Motherboard resources
00000030-00000031	Programmable interrupt controller
00000034-00000035	Programmable interrupt controller
00000038-00000039	Programmable interrupt controller
0000003C-0000003D	Programmable interrupt controller
00000040-00000043	System timer
00000044-0000005F	Motherboard resources
0000004E-0000004F	Motherboard resources
00000050-00000053	System timer
00000060-00000060	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
00000061-00000061	Motherboard resources
00000063-00000063	Motherboard resources
00000064-00000064	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
00000065-00000065	Motherboard resources
00000067-00000067	Motherboard resources
00000070-00000070	Motherboard resources
00000070-00000077	System CMOS/real time clock

00000072-0000007F	Motherboard resources
00000080-00000080	Motherboard resources
00000080-00000080	Motherboard resources
00000081-00000091	Direct memory access controller
00000084-00000086	Motherboard resources
00000088-00000088	Motherboard resources
0000008C-0000008E	Motherboard resources
00000090-0000009F	Motherboard resources
00000092-00000092	Motherboard resources
00000093-0000009F	Direct memory access controller
000000A0-000000A1	Programmable interrupt controller
000000A2-000000BF	Motherboard resources
000000A4-000000A5	Programmable interrupt controller
000000A8-000000A9	Programmable interrupt controller
000000AC-000000AD	Programmable interrupt controller
000000B0-000000B1	Programmable interrupt controller
000000B2-000000B3	Motherboard resources
000000B4-000000B5	Programmable interrupt controller
000000B8-000000B9	Programmable interrupt controller
000000BC-000000BD	Programmable interrupt controller
000000C0-000000DF	Direct memory access controller
000000E0-000000EF	Motherboard resources
000000F0-000000FF	Numeric data processor
00000274-00000277	ISAPNP Read Data Port
00000279-00000279	ISAPNP Read Data Port
00000290-0000029F	Motherboard resources
000002F8-000002FF	Communications Port (COM2)
00000378-0000037F	Printer Port (LPT1)
000003B0-000003BB	Intel(R) HD Graphics Family
000003C0-000003DF	Intel(R) HD Graphics Family
000003F0-000003F5	Standard floppy disk controller

000003F7-000003F7	Standard floppy disk controller
000003F8-000003FF	Communications Port (COM1)
00000400-00000453	Motherboard resources
00000454-00000457	Motherboard resources
00000458-0000047F	Motherboard resources
000004D0-000004D1	Motherboard resources
000004D0-000004D1	Programmable interrupt controller
00000500-0000057F	Motherboard resources
00000680-0000069F	Motherboard resources
00000778-0000077F	Motherboard resources
00000A79-00000A79	ISAPNP Read Data Port
00000B78-00000B7F	Motherboard resources
00000D00-0000FFFF	PCI bus
00000F78-00000F7F	Motherboard resources
00001000-0000100F	Motherboard resources
0000164E-0000164F	Motherboard resources
0000D000-0000D01F	Intel(R) 82583V Gigabit Network Connection
0000D000-0000DFFF	Intel(R) 6 Series/C200 Series Chipset Family PCI Express Root Port 4 – 1C16
0000E000-0000E00F	Standard Dual Channel PCI IDE Controller
0000E000-0000EFFF	Intel(R) 6 Series/C200 Series Chipset Family PCI Express Root Port 3 – 1C14
0000E010-0000E013	Standard Dual Channel PCI IDE Controller
0000E020-0000E027	Standard Dual Channel PCI IDE Controller
0000E030-0000E033	Standard Dual Channel PCI IDE Controller
0000E040-0000E047	Standard Dual Channel PCI IDE Controller
0000F000-0000F03F	Intel(R) HD Graphics Family
0000F040-0000F05F	Intel(R) 6 Series/C200 Series Chipset Family SMBus Controller – 1C22
0000F060-0000F06F	Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller – 1C09

0000F070-0000F07F	Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller – 1C09
0000F080-0000F083	Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller – 1C09
0000F090-0000F097	Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller – 1C09
0000F0A0-0000F0A3	Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller – 1C09
0000F0B0-0000F0B7	Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller – 1C09
0000F0C0-0000F0CF	Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller – 1C01
0000F0D0-0000F0DF	Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller – 1C01
0000F0E0-0000F0E3	Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller – 1C01
0000F0F0-0000F0F7	Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller – 1C01
0000F100-0000F103	Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller – 1C01
0000F110-0000F117	Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller – 1C01
0000FFFF-0000FFFF	Motherboard resources
0000FFFF-0000FFFF	Motherboard resources

Appendix B: BIOS Memory Map

Address	Device Description
000A0000-000BFFFF	Intel(R) HD Graphics Family
000A0000-000BFFFF	PCI bus
000D0000-000D3FFF	PCI bus
000D4000-000D7FFF	PCI bus
000D8000-000DBFFF	PCI bus
000DC000-000DFFFF	PCI bus
000E0000-000E3FFF	PCI bus
000E4000-000E7FFF	PCI bus
20000000-201FFFFF	System board
40000000-401FFFFF	System board
DFA00000-DFA00FFF	Motherboard resources
DFA00000-FEAFFFFF	PCI bus
E0000000-EFFFFFFF	Intel(R) HD Graphics Family
F7800000-F7BFFFFF	Intel(R) HD Graphics Family
F7C00000-F7CFFFFF	Intel(R) 82583V Gigabit Network Connection
F7C00000-F7DFFFFF	Intel(R) 6 Series/C200 Series Chipset Family PCI Express Root Port 4 -1C16
F7D00000-F7D1FFFF	Intel(R) 82583V Gigabit Network Connection
F7D20000-F7D23FFF	Intel(R) 82583V Gigabit Network Connection
F7E00000-F7EFFFFF	Intel(R) 6 Series/C200 Series Chipset Family PCI Express Root Port 3 -1C14
F7F00000-F7F03FFF	Microsoft UAA Bus Driver for High Definition Audio
F7F05000-F7F050FF	Intel(R) 6 Series/C200 Series Chipset Family SMBus Controller – 1C22
F7F06000-F7F063FF	Intel(R) 6 Series/C200 Series Chipset Family USB Enhanced Host Controller – 1C26
F7F07000-F7F073FF	Intel(R) 6 Series/C200 Series Chipset Family USB Enhanced Host Controller – 1C2D
F7F09000-F7F0900F	Intel(R) Management Engine Interface
F8000000-FBFFFFFF	Motherboard resources

FED00000-FED003FF	High precision event timer
FED10000-FED17FFF	Motherboard resources
FED18000-FED18FFF	Motherboard resources
FED19000-FED19FFF	Motherboard resources
FED1C000-ED1FFFF	Motherboard resources
FED20000-FED3FFFF	Motherboard resources
FED40000-FED44FFF	System board
FED45000-FED8FFFF	Motherboard resources
FED90000-FED93FFF	Motherboard resources
FEE00000-FEEFFFFF	Motherboard resources
FF000000-FFFFFFFF	Intel(R) 82802 Firmware Hub Device
FF000000-FFFFFFFF	Motherboard resources

Appendix C: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
ISA 0	System timer
ISA 1	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
ISA 3	Communications Port (COM2)
ISA 4	Communications Port (COM1)
ISA 6	Standard floppy disk controller
ISA 8	System CMOS/real time clock
ISA 9	Microsoft ACPI-Compliant System
ISA 12	Microsoft PS/2 Mouse
ISA 13	Numeric data processor
PCI 11	Intel(R) 6 Series/C200 Series Chipset Family SMBus Controller – 1C22
PCI 16	2nd generation Intel(R) Core(TM) processor family PCI Express Controller-0101
PCI 16	Intel(R) 6 Series/C200 Series Chipset Family PCI Express Root Port 1 – 1C10

PCI 16	Intel(R) 6 Series/C200 Series Chipset Family USB Enhanced Host Controller – 1C2D
PCI 16	Intel(R) HD Graphics Family
PCI 16	Intel(R) Management Engine Interface
PCI 17	Intel(R) 6 Series/C200 Series Chipset Family PCI Express Root Port 2 – 1C12
PCI 18	Intel(R) 6 Series/C200 Series Chipset Family PCI Express Root Port 3 – 1C14
PCI 18	Standard Dual Channel PCI IDE Controller
PCI 19	Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller – 1C09
PCI 19	Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller – 1C01
PCI 19	Intel(R) 6 Series/C200 Series Chipset Family PCI Express Root Port 4 – 1C16
PCI 19	Intel(R) 82583V Gigabit Network Connection
PCI 22	Microsoft UAA Bus Driver for High Definition Audio
PCI 23	Intel(R) 6 Series/C200 Series Chipset Family USB Enhanced Host Controller – 1C26

Appendix D: Digital I/O Setting

Below are the source codes written in C, please take them for Digital I/O application examples. The default I/O address is 6Eh.

C Language Code

```
//==== History ====//
//compile by TCPP 3.0
//R00     5/18/2010          1st modify

//#include “ring1726.h”
#include <stdio.h>
#include <dos.h>
#include <conio.h>

#define EC_CMD_Port                0x6C
#define  EC_DATA_Port    0x68
```

```
unsigned long Process_686C_Command_Write(unsigned long m_ECCMD, unsigned
long m_ECDATA);
unsigned long Process_686C_Command_Read(unsigned long m_ECCMD );
unsigned long ECU_Write_686C_RAM_BYTE( unsigned long
ECUMemAddr,unsigned long ECUMemData );
unsigned long ECU_Read_686C_RAM_BYTE( unsigned long ECUMemAddr );
unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int REG_INDEX);
void SMB_Byte_WRITE(int SMPORT, int DeviceID, int REG_INDEX, int REG_DATA);



char APName[]=      "\t\tFintek F75111 DIO LED TEST Program\n"
                    "\t=========================================\n" ;

char APHelp[]=    "\n - Pass 'A' key for inver state of DIO GP1x"
                            "\n - Pass 'S' key for inver state of DIO GP2x"
                            "\n - Pass 'D' key for inver state of DIO GP3x"
                    "\n - Pass 'Esc' key for Exit"
                    "\n" ;

void main(void){
        char getkey = 0;
    //  char DIOSTS=0;
    //  char tempJ=0;
    //  char tempA=0;
        unsigned char GP2xVal,GP3xVal,GP1xVal;
        int SMB_PORT_AD  = 0xF040;
        //--int SMB_DEVICE_ADD = 0x9C;  /*75111R's Add=6eh */
        int SMB_DEVICE_ADD = 0x6E;      /*75111R's Add=6eh */

        clrscr();  //clear screen
        printf(APName);
        printf(APHelp);

        //pg DIO as output
        //0:input 1:Output
/*      Index 10, GPIO1x Output pin control             */
        SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x10,0xff);
        delay(10);
/*      Index 20, GPIO2x Output pin control             */
//poweron defalult 0x00::::  SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_
ADD,0x20,0x00); //pg as Input
        SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x20,0xff);
/*      Index 40, GPIO3x Output pin control             */
        SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x40,0x0f);
```

```
        delay(10);

        //pg DIO default LOW
/*      Index 11, GPIO1x Output Data value          */
        SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0x00);
        GP1xVal = 0;
        delay(10);

/*      Index 21, GPIO2x Output Data value          */
        SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x21,0x00);
        GP2xVal = 0;
        delay(10);

/*      Index 41, GPIO3x Output Data value          */
        SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x41,0x00);
        GP3xVal = 0;

        gotoxy(1,9);
        //printf("DIO Status: Low \n");

        do{
                if (getkey != 27){
                        while (!kbhit());
                        getkey = getch();
                        switch (getkey){
                                case 'D':
                                case 'd':
                                                if (GP3xVal == 0)
                                                {
                                                        GP3xVal = 1; //DIO all
high
                                                        //pg DIO high
                                                        SMB_Byte_
WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x41,0x0f);

                                                        gotoxy(1,10);
                                                        printf("GP3x Status:
LED OFF\n");

                                                }
                                                else
                                                {
                                                        GP3xVal = 0; //DIO all
low
                                                        //pg DIO LOW
```

```
                                                SMB_Byte_
WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x41,0x00);

                                                gotoxy(1,10);
                                                printf("GP3x Status:
LED ON \n");
                                        }

                                        break;
                                case 'A':
                                case 'a':
                                        if (GP1xVal == 0)
                                        {
                                                GP1xVal = 1; //DIO all
high
                                                //pg DIO high
                                                SMB_Byte_
WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0xff);

                                                gotoxy(1,8);
                                                printf("GP1x Status:
LED OFF\n");

                                        }
                                        else
                                        {
                                                GP1xVal = 0; //DIO all
low
                                                //pg DIO LOW
                                                SMB_Byte_
WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0x00);

                                                gotoxy(1,8);
                                                printf("GP1x Status:
LED ON \n");
                                        }
                                        break;
                                case 'S':
                                case 's':
                                        if (GP2xVal == 0)
                                        {
                                                GP2xVal = 1; //DIO all
high
                                                //pg DIO high
                                                SMB_Byte_
```

```
WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x21,0xff);

                                                    gotoxy(1,9);
                                                    printf("GP2x Status:
LED OFF\n");

                                                }
                                                else
                                                {
                                                    GP2xVal = 0; //DIO all
low
                                                    //pg DIO LOW
                                                    SMB_Byte_
WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x21,0x00);

                                                    gotoxy(1,9);
                                                    printf("GP2x Status:
LED ON \n");
                                                }
                                        break;
                                default:
                                        break;
                        };
                        //-printf( "Input: [%c]       ", getkey);  //DEBUG
                };
        }while (getkey != 27); //ESC ascii==27
        //pg all DIO as Input
}


unsigned long Process_686C_Command_Write(unsigned long m_ECCMD, unsigned
long m_ECDATA)
{
 //---------------------------------------------------------------------------
 int     i,temp;
 unsigned long m_OutBuf;
 //---------------------------------------------------------------------------
 m_OutBuf=inportb(0x6C);
 if ( ( m_OutBuf&0x00000003) > 0 )
   {
     // temp=inportb(0x68);
     return 0xFFFFFFFF;
    }

 outport(0x6C,m_ECCMD);
```

```
 for ( i=0; i<=4000; i++ )
 {
    m_OutBuf=inportb(0x6C);
    if ( ( m_OutBuf&0x00000002) == 0 )  break;
 }
  if ( i < 3999 )
     {
       outport(0x68,m_ECDATA);
        for ( i=0; i<=4000; i++ )
        {
          m_OutBuf=inportb(0x6C);
          if ( ( m_OutBuf&0x00000002) == 0 )
                {    return 0x00000000;  }
         }
     }

 if ( i > 3999 )   m_OutBuf=inportb(0x68);
 return 0xFFFFFFFF;
}
//---------------------------------------------------------------------------
unsigned long Process_686C_Command_Read(unsigned long m_ECCMD )
{
int i,temp;
 unsigned long m_OutBuf,m_InBuf;
 m_OutBuf=inportb(0x6C);
if ( ( m_OutBuf&0x00000003) > 0 )
    {
       temp=inportb(0x68);
       return 0xFFFFFFFF;

     }
 m_InBuf = m_ECCMD;
 outport(0x6C,m_InBuf);
 for ( i=0; i<=3500; i++ )
 {
    m_OutBuf=inportb(0x6C);
   if ( ( m_OutBuf&0x00000001) > 0 )
    {
      temp=inportb(0x68);
      temp= (temp & 0x000000FF ) ;
      return temp;
     // break;
    }
 }
 if ( i > 3499 )
```

```
    {
    temp=inportb(0x68);
    return 0xFFFFFFFF;
     }
 return 0xFFFFFFFF;
 }

//---------------------------------------------------------------------------
 unsigned long ECU_Read_686C_RAM_BYTE( unsigned long ECUMemAddr )
{
  unsigned long uDATA1,uDATA2,ECRamAddrH,ECRamAddrL;
  ECRamAddrL=ECUMemAddr%256;   ECRamAddrH=ECUMemAddr/256;
  //
  uDATA1=Process_686C_Command_Write(0x000000A3, ECRamAddrH );
  if ( uDATA1==0xFFFFFFFF ) { return 0xFFFFFFFF; }
  //
  uDATA1=Process_686C_Command_Write(0x000000A2, ECRamAddrL );
  if ( uDATA1==0xFFFFFFFF ) { return 0xFFFFFFFF; }
  //
  uDATA1=Process_686C_Command_Read( 0x000000A4 );
  if ( uDATA1 > 0x000000FF ) { return 0xFFFFFFFF; }
  uDATA2=Process_686C_Command_Read( 0x000000A4 );
  if ( uDATA2 > 0x000000FF ) { return 0xFFFFFFFF; }
  if (uDATA1==uDATA2) return uDATA1;
  else return  0xFFFFFFFF;
}
//---------------------------------------------------------------------------
 unsigned long ECU_Write_686C_RAM_BYTE( unsigned long
ECUMemAddr,unsigned long ECUMemData )
{
  unsigned long uDATA, RD_DATA, ECRamAddrH, ECRamAddrL;
  ECRamAddrL=ECUMemAddr%256;   ECRamAddrH=ECUMemAddr/256;
  //
  uDATA=Process_686C_Command_Write(0x000000A3, ECRamAddrH );
  if ( uDATA==0xFFFFFFFF ) { return 0xFFFFFFFF;}
  //
  uDATA=Process_686C_Command_Write(0x000000A2, ECRamAddrL );
  if ( uDATA==0xFFFFFFFF ) { return 0xFFFFFFFF;}
  //
  uDATA=Process_686C_Command_Write(0x000000A5, ECUMemData );
  if ( uDATA==0xFFFFFFFF ) { return 0xFFFFFFFF;}
  //
  return  0x00000000;
}
//---------------------------------------------------------------------------
```

```
unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int REG_INDEX)
{
        unsigned char SMB_R;
        outportb(SMPORT+02, 0x00);      /* clear */
        outportb(SMPORT+00, 0xff);      /* clear */
        delay(10);
        outportb(SMPORT+04, DeviceID+1);    /* clear */
        outportb(SMPORT+03, REG_INDEX);     /* clear */
        outportb(SMPORT+02, 0x48);      /* read_byte */
        delay(10);
        //printf(" %02x ",inportb(SMPORT+05));
        SMB_R= inportb(SMPORT+05);
        return SMB_R;
}

void SMB_Byte_WRITE(int SMPORT, int DeviceID, int REG_INDEX, int REG_DATA)
{
        outportb(SMPORT+02, 0x00);      /* clear */
        outportb(SMPORT+00, 0xff);      /* clear */
        delay(10);
        outportb(SMPORT+04, DeviceID);          /* clear */
        outportb(SMPORT+03, REG_INDEX);         /* clear */
        outportb(SMPORT+05, REG_DATA);          /* read_byte */
        outportb(SMPORT+02, 0x48);      /* read_byte */
/*      delay(10);
        printf(" %02x ",inportb(SMPORT+05)); */
}
```