EmETXe-i67M2
EmETXe-i65M2

COM Express Type 6 CPU Module

User's Manual

Version 1.0

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Chapter 1

Introduction

1.1 Copyright Notice

All Rights Reserved.

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

1.2 Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

> Warning
>
> This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

1.3 About This User's Manual

This user's manual provides general information and installation instructions about the product. This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. please consult your vendor before further handling.

1.4 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

1.5 Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

1.6 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw

E-mail:info@arbor.com.tw

1.7 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

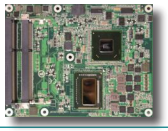
Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.8 Packing List

Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:



1 x EmETXe-i67M2/ i65M2 COM Express CPU Module

1 x Driver CD

1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

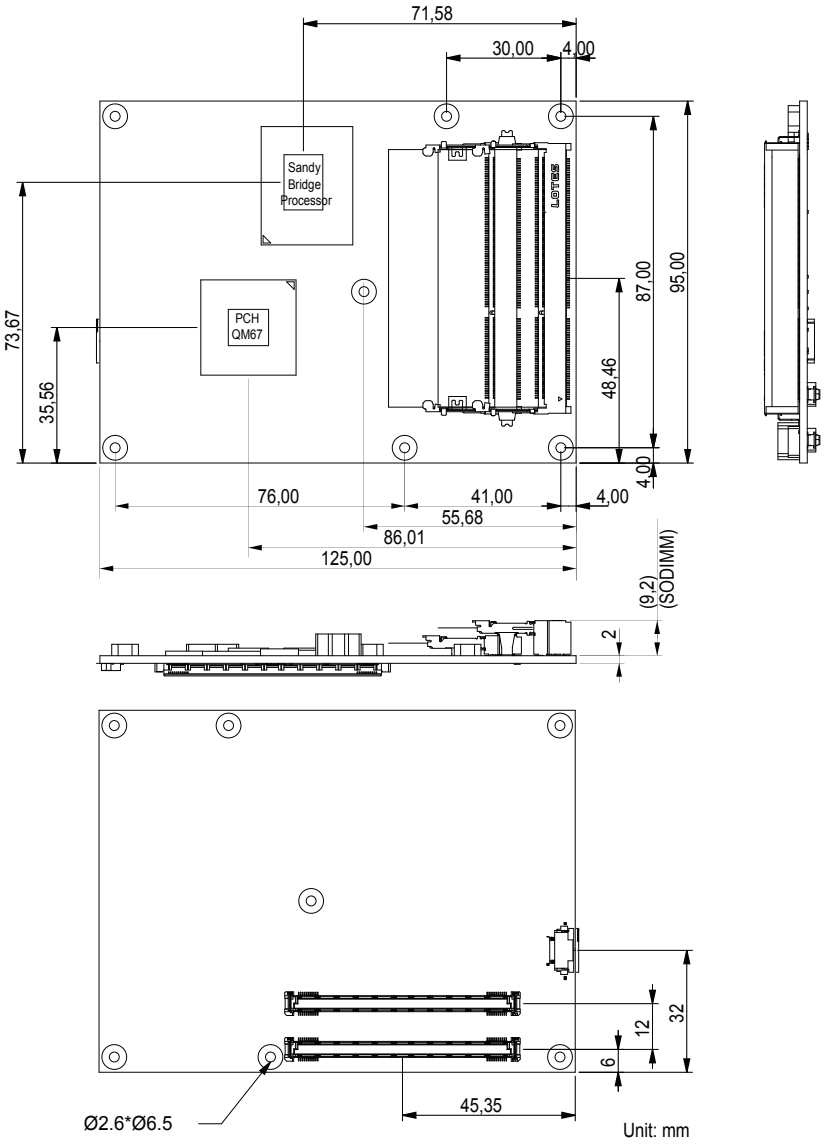
1.9 Ordering Information

EmETXe-i67M2-2610UE	Intel® i7-2610UE COM Express CPU module
EmETXe-i65M2-827E	Intel® Celeron 827E COM Express CPU module
HS-65M2-F1	Heat Spreader (95 x 125 x 18mm)
HS-65M2-C1	Cooler (95 x 125 x 34.8mm)
PBE-1702	COM Express Type 6 evaluation board in ATX form factor
CBK-04-1702-00	Cable kit 1 x SATA cable 2 x COM port cables 1 x USB cable

1.10 Specifications

Form Factor	COM Express Type 6 CPU Module
CPU	Intel® Core™ i7-2610UE 1.5GHz or Celeron™ 827E 1.4GHz processors
Chipset	Intel® QM67 for EmETXe-i67M2-2610UE Intel® HM65 for EmETXe-i65M2-827E
System Memory	2 x DDR3 SO-DIMM sockets, supporting up to 8GB SDRAM
VGA/ LCD Controller	Intel® Graphics Media Accelerator 3000 graphics core w/ Analog RGB/ Dual Channels 24-bit LVDS (Dual independent displays), 3 x DDI ports
Ethernet controller	1 x Intel 82579LM Gigabit Ethernet PHY
BIOS	AMI PnP Flash BIOS
Storage	2 x Serial ATA ports w/ 600MB/s HDD transfer rate 2 x Serial ATA ports w/ 300MB/s HDD transfer rate
Parallel Port	SPP/EPP/ECP mode selectable (via COM Express carrier board)
Universal Serial Bus	8 x USB 2.0 ports
LCD	Dual Channels 24-bit LVDS
Expansion Interface	1 x PCIe x16 lanes 7 x PCIe x1 lanes SPI, and LPC (Low Pin Count) interface
Operation Temp.	-20ºC ~ 70ºC (-4ºF ~ 158ºF)
Watchdog Timer	1~ 255 levels Reset
Dimension (L x W)	125 x 95 mm (4.9” x 3.7”)

1.11 Board Dimensions



Chapter 2

Installation

2.1 What is “COM Express”?

With more and more demands on small and embedded industrial boards, a multi-functioned COM (Computer-on-Module) is the great one of the solutions.
COM Express, board-to-board connectors consist of two rows of 220 pins each.
Row AB, which is required, provides pins for PCI Express, SATA, LVDS, LCD channel, LPC bus, system and power management, VGA, LAN, and power and ground interfaces.
Row CD, which is optional, provides SDVO and legacy PCI and IDE signals next to additional PCI Express, LAN and power and ground signals.

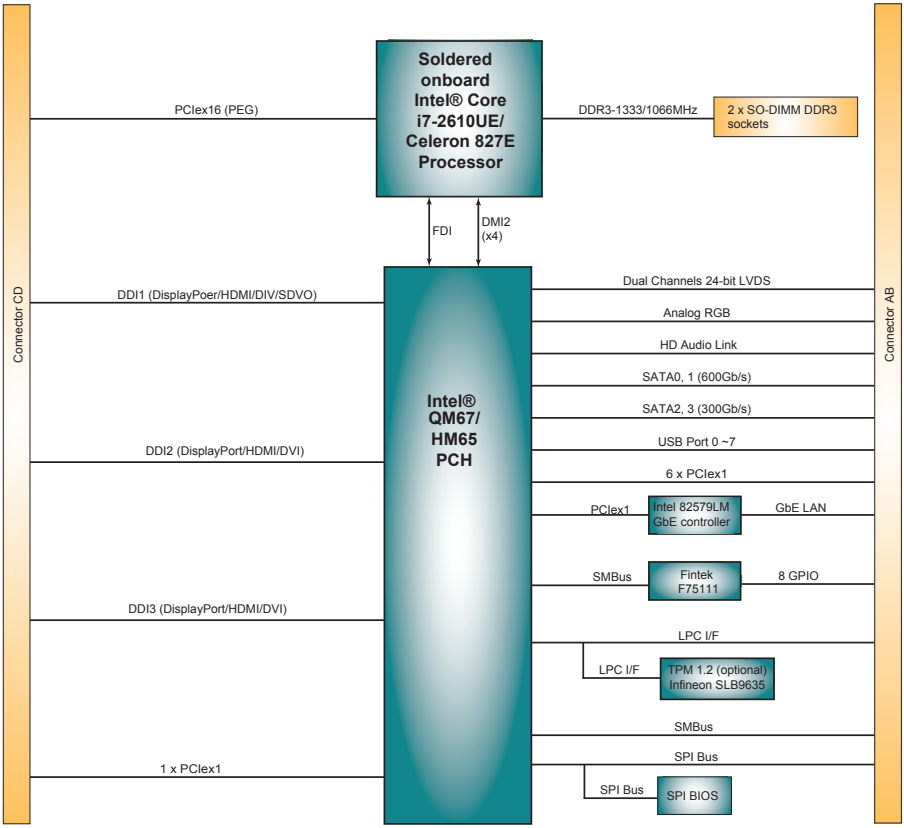
By the way, the target markets of COM will be focused on:

- Retail & Advertising
- Medical
- Test & Measurement
- Gaming & Entertainment
- Industrial & Automation
- Military & Government
- Security

COM Express supports seven pin-out Type applying to Basic and Extended form factors:
Module Type 1 and 10 support single connector with two rows of pins (220 pins) Module Type 2, 3, 4, 5 and 6 support two connectors with four rows of pins (440 pins) Connector placement and most mounting holes have transparency between Form Factors.
The differences among the Module Type 6 and EmETXe-i67M2/ EmETXe-i65M2 are summarized in table below:

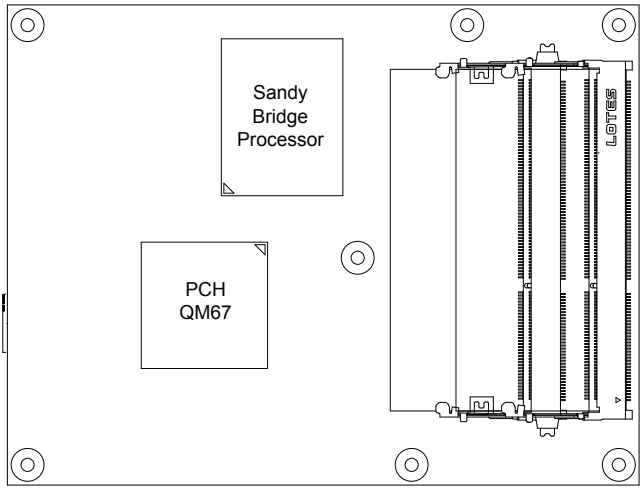
Module Type	Standard Type 6	EmETXe-i67M2	EmETXe-i65M2
Connectors	2	2	2
Connector Rows	A, B, C, D	A, B, C, D	A, B, C, D
PCIe Lanes (Max)	24	23	23
PCI Bus	No	No	No
PATA - IDE	No	No	No
LAN (Max)	1	1	1
Serial Ports (Max)	2	0	0
Muxed SDVO	No	No	No
Digital Display I/F (Max)	3	3	3
USB 3.0 Ports (Max)	4	0	0

2.2 Block Diagram



2.3 Connectors

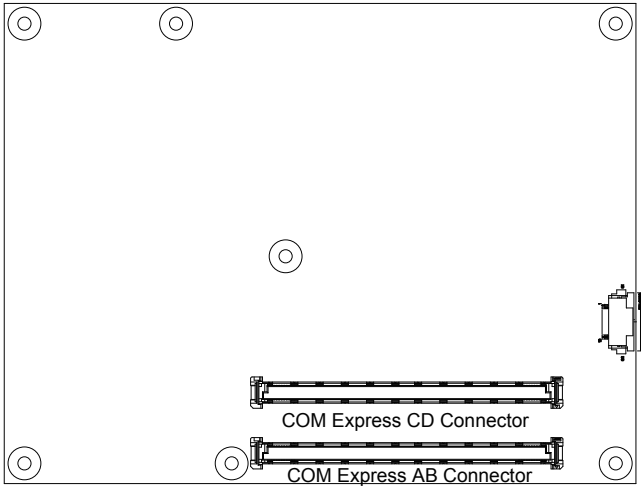
Top side



Bottom side

COM Express AB Connector

COM Express CD Connector



2.4 COM Express AB Connector (bottom side)

B1	GND (FIXED)	GND (FIXED)	A1
B2	GBE0_ACT#	GBE0_MDI3-	A2
B3	LPC_FRAME#	GBE0_MDI3+	A3
B4	LPC_AD0	GBE0_LINK100#	A4
B5	LPC_AD1	GBE0_LINK1000#	A5
B6	LPC_AD2	GBE0_MDI2-	A6
B7	LPC_AD3	GBE0_MDI2+	A7
B8	LPC_DRQ0#	GBE0_LINK#	A8
B9	LPC_DRQ1#	GBE0_MDI1-	A9
B10	LPC_CLK	GBE0_MDI1+	A10
B11	GND (FIXED)	GND (FIXED)	A11
B12	PWRBTN#	GBE0_MDI0-	A12
B13	SMB_CK	GBE0_MDI0+	A13
B14	SMB_DAT	GBE0_CTREF	A14
B15	SMB_ALERT#	SUS_S3#	A15
B16	SATA1_TX+	SATA0_TX+	A16
B17	SATA1_TX-	SATA0_TX-	A17
B18	SUS_STAT#	SUS_S4#	A18
B19	SATA1_RX+	SATA0_RX+	A19
B20	SATA1_RX-	SATA0_RX-	A20
B21	GND (FIXED)	GND (FIXED)	A21
B22	SATA3_TX+	SATA2_TX+	A22
B23	SATA3_TX-	SATA2_TX-	A23
B24	PWR_OK	SUS_S5#	A24
B25	SATA3_RX+	SATA2_RX+	A25
B26	SATA3_RX-	SATA2_RX-	A26
B27	WDT	BATLOW#	A27
B28	AC_SDIN2	ATA_ACT#	A28
B29	AC_SDIN1	AC_SYNC	A29
B30	AC_SDIN0	AC_RST#	A30
B31	GND	GND	A31
B32	SPKR	AC_BITCLK	A32
B33	I2C_CK	AC_SDOUT	A33
B34	I2C_DAT	BIOS_DISABLE#	A34
B35	THRM#	THRMTRIP#	A35
B36	USB7-	USB6-	A36
B37	USB7+	USB6+	A37
B38	USB_4_5_OC#	USB_6_7_OC#	A38
B39	USB5-	USB4-	A39
B40	USB5+	USB4+	A40
B41	GND	GND	A41
B42	USB3-	USB2-	A42
B43	USB3+	USB2+	A43
B44	USB_0_1_OC#	USB_2_3_OC#	A44
B45	USB1-	USB0-	A45
B46	USB1+	USB0+	A46
B47	EXCD1_PERST#	VCC_RTC	A47
B48	EXCD1_CPPE#	EXCD0_PERST#	A48
B49	SYS_RESET#	EXCD0_CPPE#	A49
B50	CB_RESET#	LPC_SERIRQ	A50
B51	GND	GND	A51
B52	PCIE_RX5+	PCIE_TX5+	A52
B53	PCIE_RX5-	PCIE_TX5-	A53
B54	GPO1	GPI0	A54
B55	PCIE_RX4+	PCIE_TX4+	A55

B56	PCIE_RX4-	PCIE_TX4-	A56
B57	GPO2	GND	A57
B58	PCIE_RX3+	PCIE_TX3+	A58
B59	PCIE_RX3-	PCIE_TX3-	A59
B60	GND	GND	A60
B61	PCIE_RX2+	PCIE_TX2+	A61
B62	PCIE_RX2-	PCIE_TX2-	A62
B63	GPO3	GPI1	A63
B64	PCIE_RX1+	PCIE_TX1+	A64
B65	PCIE_RX1-	PCIE_TX1-	A65
B66	WAKE0#	GND	A66
B67	WAKE1#	GPI2	A67
B68	PCIE_RX0+	PCIE_TX0+	A68
B69	PCIE_RX0-	PCIE_TX0-	A69
B70	GND	GND	A70
B71	LVDS_B0+	LVDS_A0+	A71
B72	LVDS_B0-	LVDS_A0-	A72
B73	LVDS_B1+	LVDS_A1+	A73
B74	LVDS_B1-	LVDS_A1-	A74
B75	LVDS_B2+	LVDS_A2+	A75
B76	LVDS_B2-	LVDS_A2-	A76
B77	LVDS_B3+	LVDS_VDD_EN	A77
B78	LVDS_B3-	LVDS_A3+	A78
B79	LVDS_BKLT_EN	LVDS_A3-	A79
B80	GND	GND	A80
B81	LVDS_B_CK+	LVDS_A_CK+	A81
B82	LVDS_B_CK-	LVDS_A_CK-	A82
B83	CKLVDS_BKLT_CTRL	LVDS_I2C_CK	A83
B84	VCC_5V_SBY	LVDS_I2C_DAT	A84
B85	VCC_5V_SBY	GPI3	A85
B86	VCC_5V_SBY	KBD_RST#	A86
B87	VCC_5V_SBY	KBD_A20GATE	A87
B88	RSVD	PCIE0_CK_REF+	A88
B89	VGA_RED	PCIE0_CK_REF-	A89
B90	GND	GND	A90
B91	VGA_GRN	RSVD B91	A91
B92	VGA_BLU	RSVD	A92
B93	VGA_HSYNC	GPO0	A93
B94	VGA_VSYNC	RSVD	A94
B95	VGA_I2C_CK	RSVD	A95
B96	VGA_I2C_DAT	GND	A96
B97	TV_DAC_A	VCC_12V	A97
B98	TV_DAC_B	VCC_12V	A98
B99	TV_DAC_C	VCC_12V	A99
B100	GND	GND	A100
B101	VCC_12V	VCC_12V	A101
B102	VCC_12V	VCC_12V	A102
B103	VCC_12V	VCC_12V	A103
B104	VCC_12V	VCC_12V	A104
B105	VCC_12V	VCC_12V	A105
B106	VCC_12V	VCC_12V	A106
B107	VCC_12V	VCC_12V	A107
B108	VCC_12V	VCC_12V	A108
B109	VCC_12V	VCC_12V	A109
B110	GND	GND	A110

2.5 COM Express CD Connector (bottom side)

D1	GND (FIXED)	GND (FIXED)	C1
D2	GND	GND	C2
D3	USB_SSTX0-	USB_SSRX0-	C3
D4	USB_SSTX0+	USB_SSRX0+	C4
D5	GND	GND	C5
D6	USB_SSTX1-	USB_SSRX1-	C6
D7	USB_SSTX1+	USB_SSRX1+	C7
D8	GND	GND	C8
D9	USB_SSTX2-	USB_SSRX2-	C9
D10	USB_SSTX2+	USB_SSRX2+	C10
D11	GND (FIXED)	GND (FIXED)	C11
D12	USB_SSTX3-	USB_SSRX3-	C12
D13	USB_SSTX3+	USB_SSRX3+	C13
D14	GND	GND	C14
D15	DDI1_CTRLCLK_AUX+	DDI1_PAIR6+	C15
D16	DDI1_CTRLCLK_AUX-	DDI1_PAIR6-	C16
D17	RSVD	RSVD	C17
D18	RSVD	RSVD	C18
D19	PCIE_TX6+	PCIE_RX6+	C19
D20	PCIE_TX6-	PCIE_RX6-	C20
D21	GND(FIXED)	GND(FIXED)	C21
D22	PCIE_TX7+	PCIE_RX7+	C22
D23	PCIE_TX7-	PCIE_RX7-	C23
D24	RSVD	DDI1_HPD	C24
D25	RSVD	DDI1_PAIR4+	C25
D26	DDI1_PAIR0+	DDI1_PAIR4-	C26
D27	DDI1_PAIR0-	RSVD	C27
D28	RSVD	RSVD	C28
D29	DDI1_PAIR1+	DDI1_PAIR5+	C29
D30	DDI1_PAIR1-	DDI1_PAIR5-	C30
D31	GND(FIXED)	GND (FIXED)	C31
D32	DDI1_PAIR2+	DDI2_CTRLCLK_AUX+	C32
D33	DDI1_PAIR2-	DDI2_CTRLCLK_AUX-	C33
D34	DDI1_DDC_AUX_SEL	DDI2_DDC_AUX_SEL	C34
D35	RSVD	RSVD	C35
D36	DDI1_PAIR3+	DDI3_CTRLCLK_AUX+	C36
D37	DDI1_PAIR3-	DDI3_CTRLCLK_AUX-	C37
D38	RSVD	DDI3_DDC_AUX_SEL	C38
D39	DDI1_PAIR0+	DDI3_PAIR0+	C39
D40	DDI1_PAIR0-	DDI3_PAIR0-	C40
D41	GND(FIXED)	GND(FIXED)	C41
D42	DDI1_PAIR1+	DDI3_PAIR1+	C42
D43	DDI1_PAIR1-	DDI3_PAIR1-	C43
D44	DDI2_HPD	DDI3_HPD	C44
D45	RSVD	RSVD	C45
D46	DDI2_PAIR2+	DDI3_PAIR2+	C46
D47	DDI2_PAIR2-	DDI3_PAIR2-	C47
D48	RSVD	RSVD	C48
D49	DDI2_PAIR3+	DDI3_PAIR3+	C49
D50	DDI2_PAIR3-	DDI3_PAIR3-	C50
D51	GND (FIXED)	GND (FIXED)	C51
D52	PEG_TX0+	PEG_RX0+	C52
D53	PEG_TX0-	PEG_RX0-	C53
D54	PEG_LANE_RV#	TYPE0#	C54
D55	PEG_TX1+	PEG_RX1+	C55

D56	PEG_TX1-	PEG_RX1-	C56
D57	TYPE2#	TYPE1#	C57
D58	PEG_TX2+	PEG_RX2+	C58
D59	PEG_TX2-	PEG_RX2-	C59
D60	GND (FIXED)	GND (FIXED)	C60
D61	PEG_TX3+	PEG_RX3+	C61
D62	PEG_TX3-	PEG_RX3-	C62
D63	RSVD	RSVD	C63
D64	RSVD	RSVD	C64
D65	PEG_TX4+	PEG_RX4+	C65
D66	PEG_TX4-	PEG_RX4-	C66
D67	RSVD	RSVD	C67
D68	PEG_TX5+	PEG_RX5+	C68
D69	PEG_TX5-	PEG_RX5-	C69
D70	GND (FIXED)	GND (FIXED)	C70
D71	PEG_TX6+	PEG_RX6+	C71
D72	PEG_TX6-	PEG_RX6-	C72
D73	GND	GND	C73
D74	PEG_TX7+	PEG_RX7+	C74
D75	PEG_TX7-	PEG_RX7-	C75
D76	GND	GND	C76
D77	RSVD	RSVD	C77
D78	PEG_TX8+	PEG_RX8+	C78
D79	PEG_TX8-	PEG_RX8-	C79
D80	GND (FIXED)	GND (FIXED)	C80
D81	PEG_TX9+	PEG_RX9+	C81
D82	PEG_TX9-	PEG_RX9-	C82
D83	RSVD	RSVD	C83
D84	GND	GND	C84
D85	PEG_TX10+	PEG_RX10+	C85
D86	PEG_TX10-	PEG_RX10-	C86
D87	GND	GND	C87
D88	PEG_TX11+	PEG_RX11+	C88
D89	PEG_TX11-	PEG_RX11-	C89
D90	GND (FIXED)	GND (FIXED)	C90
D91	PEG_TX12+	PEG_RX12+	C91
D92	PEG_TX12-	PEG_RX12-	C92
D93	GND	GND	C93
D94	PEG_TX13+	PEG_RX13+	C94
D95	PEG_TX13-	PEG_RX13-	C95
D96	GND	GND	C96
D97	RSVD	RSVD	C97
D98	PEG_TX14+	PEG_RX14+	C98
D99	PEG_TX14-	PEG_RX14-	C99
D100	GND (FIXED)	GND (FIXED)	C100
D101	PEG_TX15+	PEG_RX15+	C101
D102	PEG_TX15-	PEG_RX15-	C102
D103	GND	GND	C103
D104	VCC_12V	VCC_12V	C104
D105	VCC_12V	VCC_12V	C105
D106	VCC_12V	VCC_12V	C106
D107	VCC_12V	VCC_12V	C107
D108	VCC_12V	VCC_12V	C108
D109	VCC_12V	VCC_12V	C109
D110	GND (FIXED)	GND (FIXED)	C110

2.6 The Installation Paths of CD Driver

Windows 2000 & XP

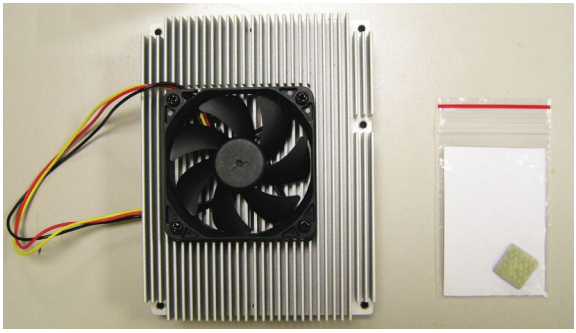
Driver	Path
CHIPSET	\EmETXe-i67M2\CHIPSET
LAN	\EmETXe-i67M2\ETHERNET\XP_WIN7_SERIES\32 \EmETXe-i67M2\ETHERNET\XP_WIN7_SERIES\64
NET Framework	\EmETXe-i67M2\NET Framework
VGA	\EmETXe-i67M2\GRAPHICS\Windows XP 32bit Graphics Drivers\Windows XP Graphics Drivers\ winxp \EmETXe-i67M2\GRAPHICS\Windows XP 64bit Graphics Drivers\Windows XP64 Graphics Drivers\ winxp64
Management Engine	\EmETXe-i67M2\ME
RAID	\EmETXe-i67M2\IRST

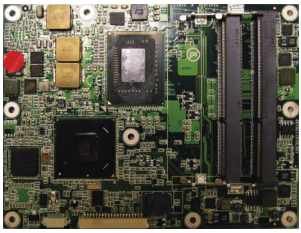
Windows 7

Driver	Path
CHIPSET	\EmETXe-i67M2\CHIPSET
LAN	\EmETXe-i67M2\ETHERNET\XP_WIN7_SERIES\32 \EmETXe-i67M2\ETHERNET\XP_WIN7_SERIES\64
VGA	\EmETXe-i67M2\GRAPHICS\Windows 7 Graphics Driver 32_bit\Windows Vista Windows 7 Graphics Driver\WinVista7 \EmETXe-i67M2\GRAPHICS\Windows 7 64-Bit Graphics Driver\Windows Vista Windows 7 64-Bit Graphics Driver\WinVista7_64
Management Engine	\EmETXe-i67M2\ME
Intel Turbo	\EmETXe-i67M2\OTHERS

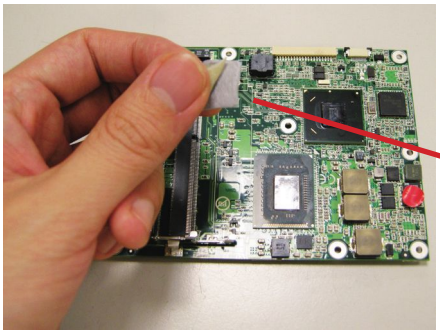
2.7 Heatsink Installation

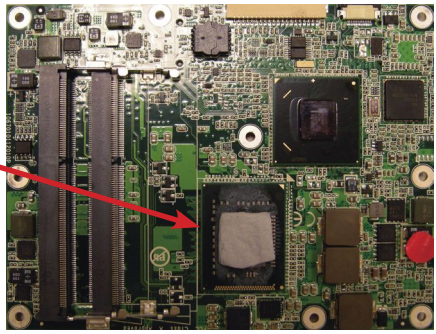
1. Prepare your optional heatsink, thermal pad and CPU module.



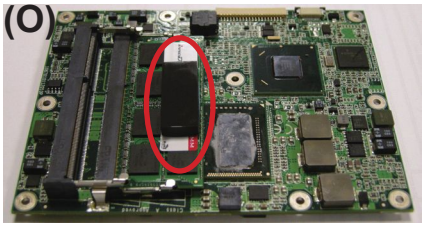


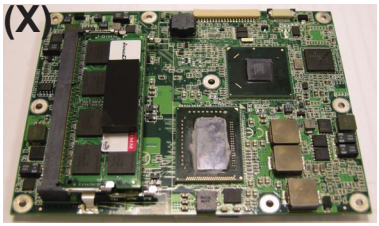
2. For EmETXe-i65M2-827E, you have to put an additional thermal pad between heatsink and CPU module, but EmETXe-i67M2-2610UE can skip this step. Please tear protective membranes on both sides from thermal pad first of all, be sure not to pinch or mold the thermal pad, and then put it as right picture.





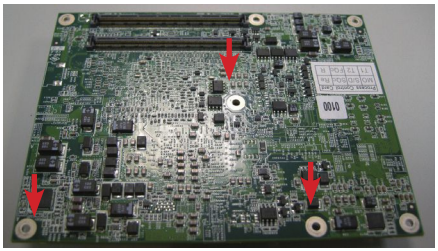
3. For both i67M2 and i65M2, you may also apply thermal pad to their memory module. But be aware to put it on the designated place of the first module, as the left illustration, and don't put it on the 2nd module, as right picture, for the 2nd memory module doesn't need it.

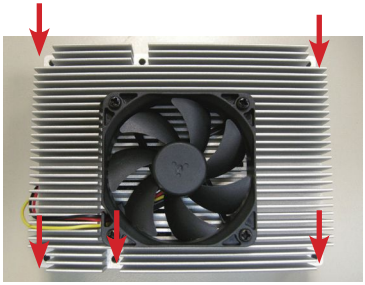




4. After everything is settled down, please assemble heatsink with CPU module according to their corresponding screw positions.

5. Carefully turn them over together and secure the first 3 screws as left picture. Overturn again to secure the rest as right picture.





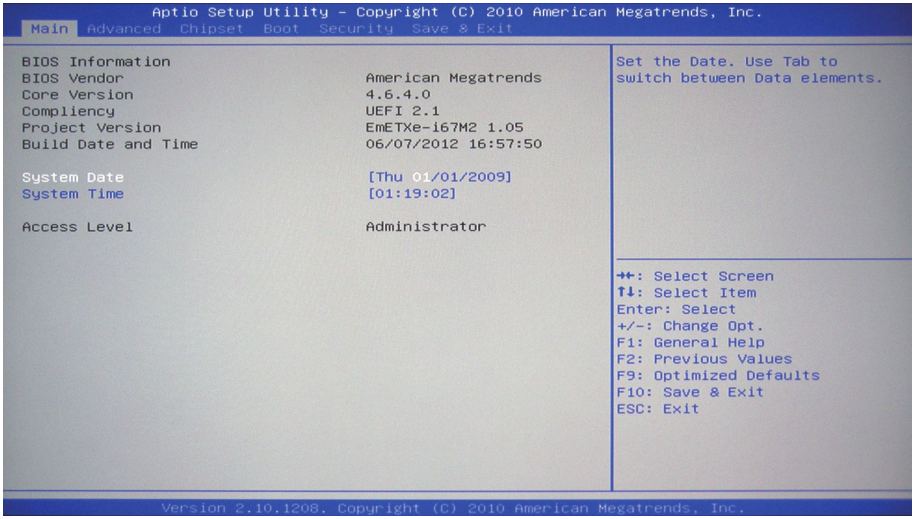
Chapter 3

BIOS

3.1 BIOS Main Setup

The AMI BIOS provides a setup utility program for specifying the system configurations and settings which are stored in the BIOS ROM of the system. When you turn on the computer, the AMI BIOS is immediately activated. After you have entered the setup utility, use the left/right arrow keys to highlight a particular configuration screen from the top menu bar or use the down arrow key to access and configure the information below.

NOTE: In order to increase system stability and performance, our engineering staff are constantly improving the BIOS menu. The BIOS setup screens and descriptions illustrated in this manual are for your reference only, and may not completely match what you see on your screen.



BIOS Information

Display the BIOS information.

System Date

Set the system date. Note that the 'Day' automatically changes when you set the date.

The date format is:

Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1999 to 2099

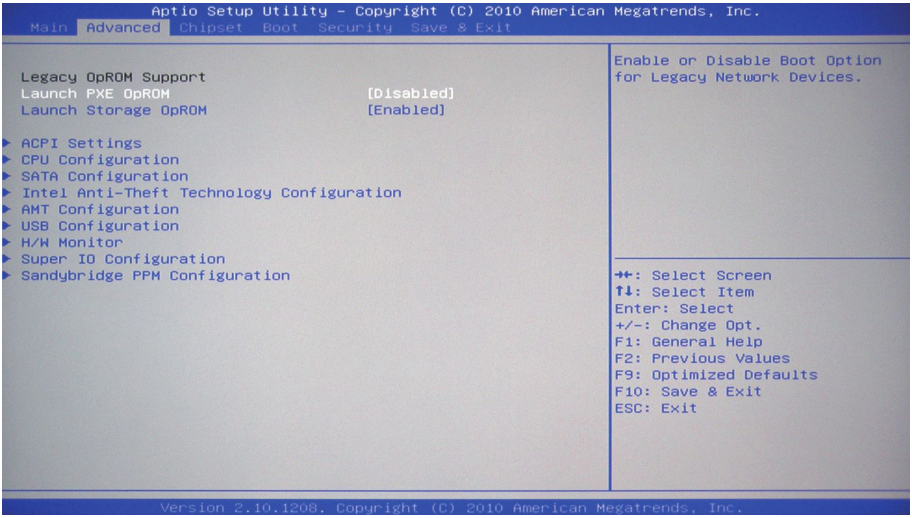
System Time

Set the system time.

The time format is:

Hour : 00 to 23
Minute : 00 to 59
Second : 00 to 59

3.2 Advanced Settings



Legacy OpROM Support

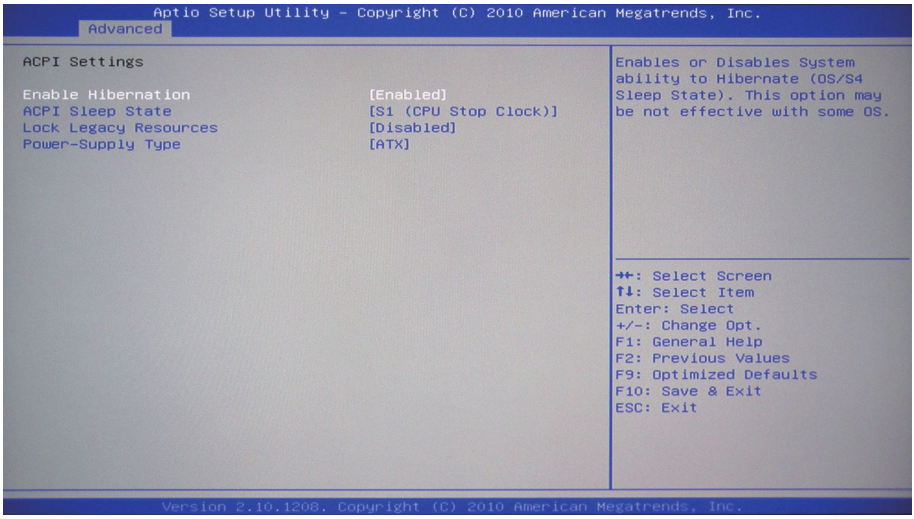
Launch PXE OpROM

Enable or disable the boot option for legacy network devices.

Launch Storage OpROM

Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

3.2.1 ACPI Configuration



Enable Hibernation
Enable or disable System ability to Hibernation (OS/S4 Sleep State). This option may be not effective with some OS.

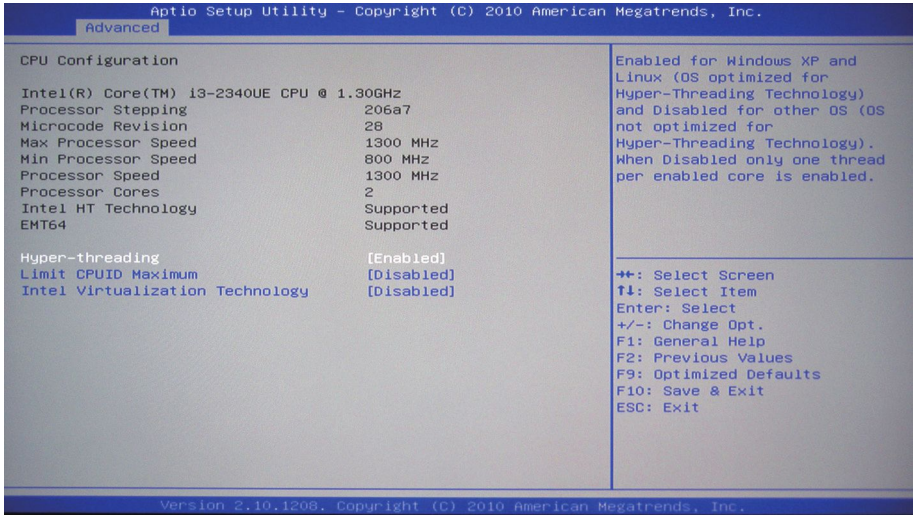
ACPI Sleep State
Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
The choice: Suspend Disabled, S1 (CPU Stop Clock), S3 (Suspend to RAM)

Lock Legacy Resources
Enable or disable Lock of Legacy Resources.

Power-Supply Type
Set power-supply type.
The choice: AT, ATX

3.2.2 CPU Configuration

The CPU Configuration setup screen varies depending on the installed processor.



Hyper-threading

This item is used to enable or disable the processor's Hyper-threading feature.

Enabled for Windows XP and Linux (OS optimized for Hyper-threading Technology) and disabled for other OS (OS not optimized for Hyper-threading Technology).

When disabled, only one thread per enabled core is enabled.

Limit CPUID Maximum

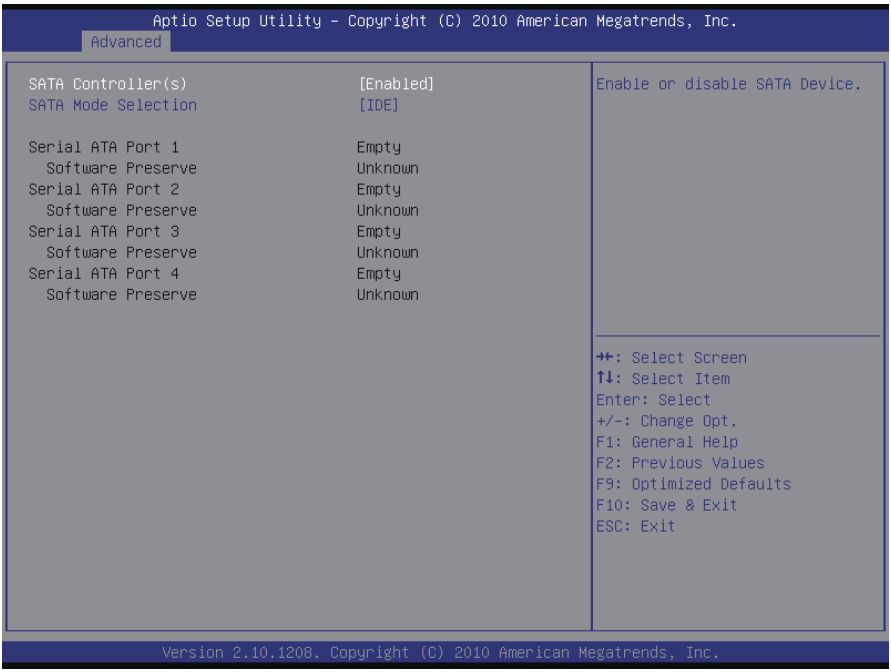
Enable or disable the Limit CPUID Maximum.

Intel Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

3.2.3 SATA Configuration

It allows you to select the operation mode for SATA controller.



SATA Controller(s)

Enable or disable SATA devices.

SATA Mode Selection

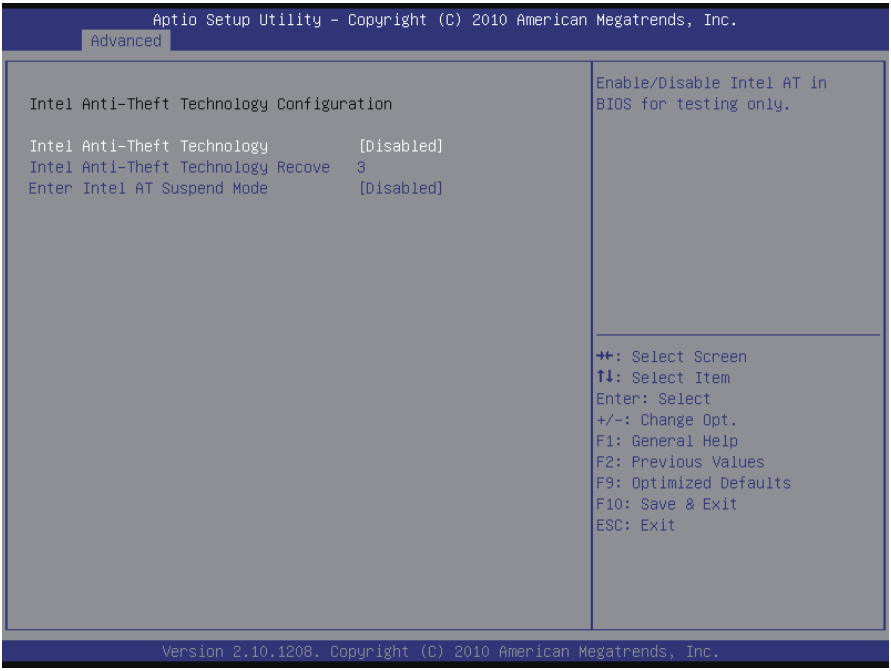
The choice: Disable; IDE (Default), AHCI (not available in EmETXe-i65M2), RAID

IDE: Set the Serial ATA drives as Parallel ATA storage devices.

AHCI: Allow the Serial ATA devices to use AHCI (Advanced Host Controller Interface).

RAID: Create RAID or Intel Matrix Storage configuration on Serial ATA devices.

3.2.4 Intel Anti-Theft Technology Configuration



Intel Anti-Theft Technology

Enable or disable Intel® Anti-Theft Technology function in BIOS.

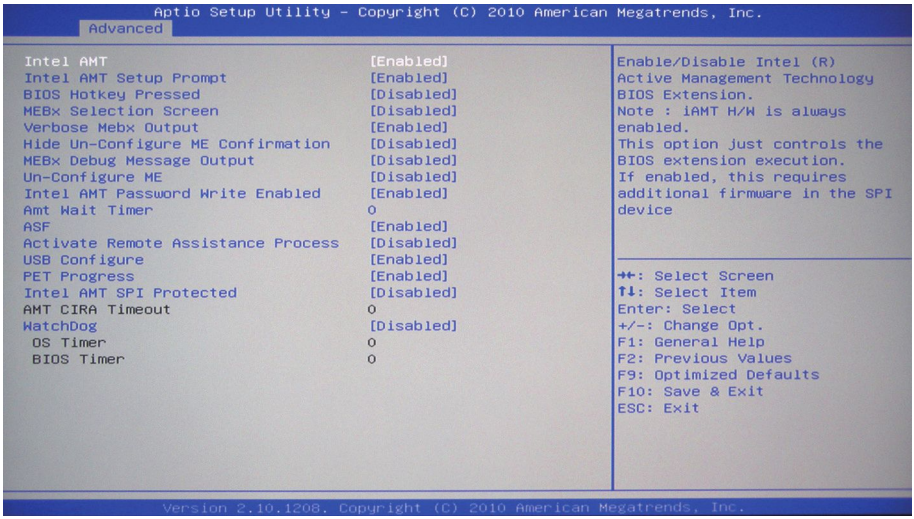
Intel Anti-Theft Technology Recovery

Set the number of times Recovery attempted will be allowed.

Enter Intel AT Suspend Mode

Enable or disable the request that platform enters AT suspend mode.

3.2.5 AMT Configuration



Intel AMT (not available in EmETXe-i65M2)

Enable/Disable Intel® Active Management Technology BIOS Extension. NOTE: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

Intel AMT Setup Prompt

OEMFLag Bit 0:
Enable/Disable Intel AMT Setup Prompt to wait for hot-key to enter setup.

BIOS Hotkey Pressed

OEMFLag Bit 1:
Enable/Disable BIOS hotkey press.

MeBx Selection Screen

OEMFLag Bit 2:
Enable/Disable MEBx selection screen.

Verbose Mebx Output

OEMFLag Bit 3:
Enable/Disable Verbose Mebx Output.

Hide Un-Configure ME Confirmation

OEMFLag Bit 6:
Hide Un-Configure ME without password Confirmation Prompt.

MeBx Debug Message Output

OEMFLag Bit 14:
Enable MEBx debug message output.

Un-Configure ME

OEMFLag Bit 15:
Un-Configure ME without password.

Intel AMT Password Write Enabled

Enable/Disable Intel AMT Password Write. Password is writable when set Enable.

Amt Wait Timer

Set timer to wait before sending ASF_GET_BOOT_OPTIONS.

ASF

Enable/Disable Alert Specification Format.

Activate Remote Assistance Process

Trigger CIRA boot.

USB Configure

Enable/Disable USB Configure function.

PET Progress

User can enable/disable PET Events progress to received PET events or not.

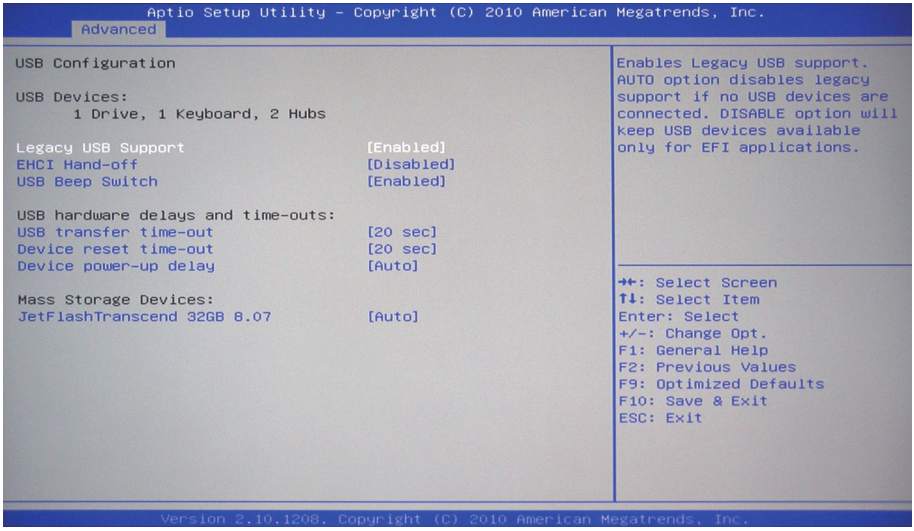
Intel Amt SPI Protected

Enable/Disable Intel AMT SPI write protect.

WatchDog

Enable/Disable WatchDog Timer.

3.2.6 USB Configuration



Legacy USB Support

Enable support for legacy USB. AUTO option disables legacy support if no USB devices are connected.
The choice: Enabled (Default); Auto; Disabled

EHCI Hand-off

Allow you to enable support for operating systems without an EHCI hand-off feature. Do not disable the BIOS EHCI Hand-Off option if you are running a Windows® operating system with USB device.
The choice: Enabled (Default); Disabled

USB Beep Switch

Enable/Disable USB Beep sound.

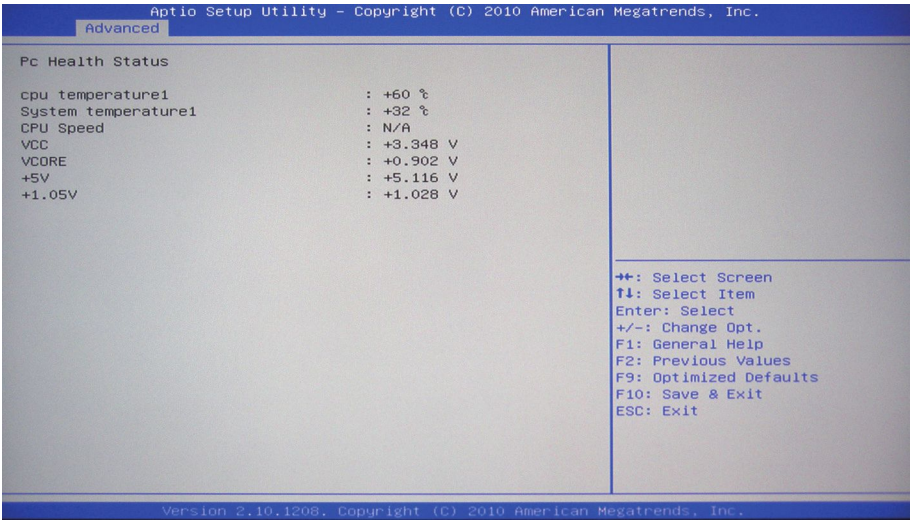
USB hardware delays and time-outs

USB transfer time-out — The time-out value for control, bulk, and interrupt transfers. Default setting: 20 sec
Device reset time-out — USB mass storage device start unit command time-out. Default setting: 20 sec
Device power-up delay — Maximum time the device will take before it properly reports itself to the host controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from hub descriptor. The choice: Auto (Default); Manual

Mass Storage Devices

This item displays information when USB devices are detected.

3.2.7 H/W Monitor

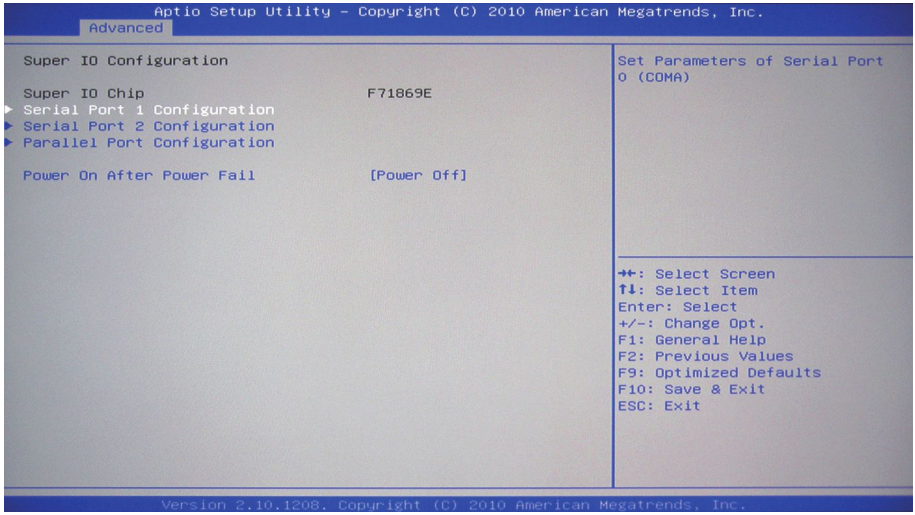


PC Health Status

The hardware monitor menu shows the operating temperature and system voltages of CPU module.

3.2.8 Super IO Configuration

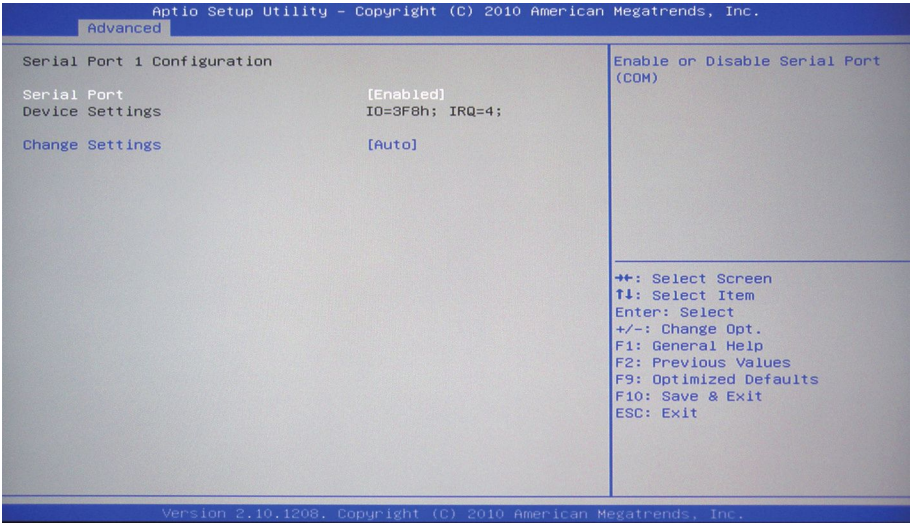
You can use this item to set up or change the Super IO configuration for FDD controllers, parallel ports and serial ports.



Power On After Power Failure

Specify what state to go to when power is re-applied after a power failure.

Serial Port 1~2 Configuration



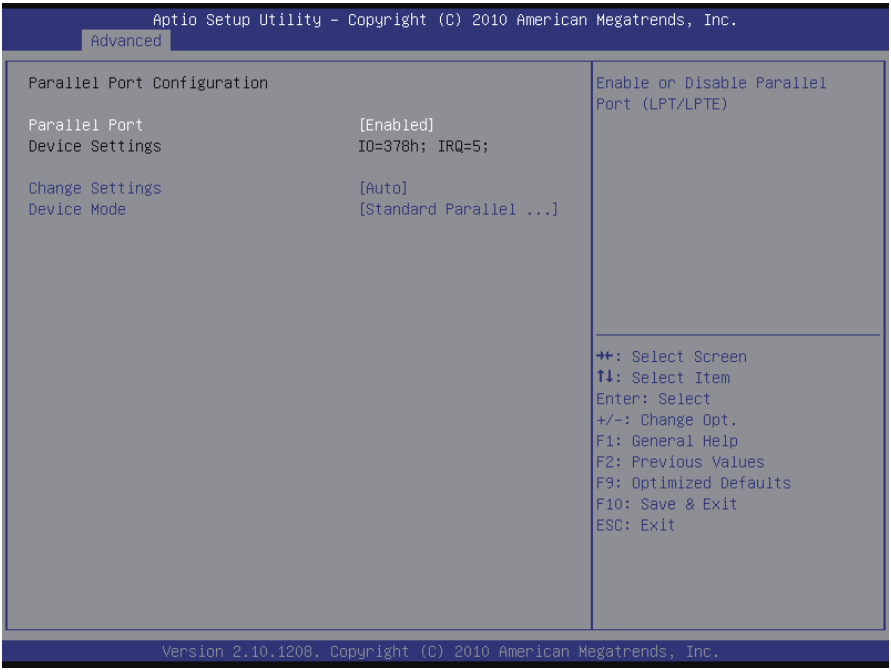
Serial Port

Use the Serial port option to enable or disable the serial port.
The choice: Enabled, Disabled

Change Settings

Use the Change Settings option to change the serial port's IO port address and interrupt address.
The choice:
Auto
IO=3F8h; IRQ=4,
IO=3F8h; IRQ=3,4,5,6,7,10,11,12
IO=2F8h; IRQ=3,4,5,6,7,10,11,12
IO=3E8h; IRQ=3,4,5,6,7,10,11,12
IO=2E8h; IRQ=3,4,5,6,7,10,11,12

Parallel Port Configuration



Parallel Port Configuration

This item allows you to enable/disable Parallel Port (LPT/LPTE).

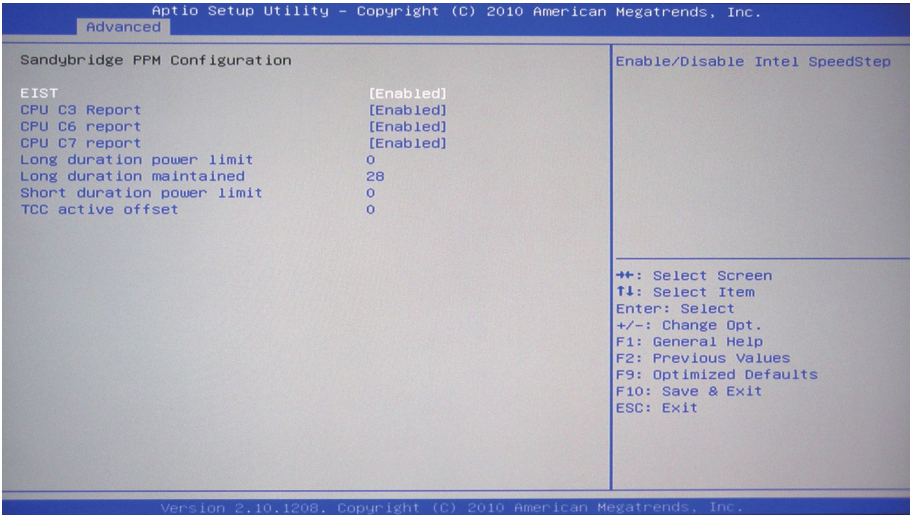
Change Settings

Use the Change Settings option to change the parallel port's IO port address and interrupt address.
The choice:
Auto
IO=378h; IRQ=5,
IO=378h; IRO=5,6,7,10,11,12,
IO=378h; IRQ=5,6,7,10,11,12,
IO=278h; IRQ=5,6,7,10,11,12,
IO=38Ch; IRQ=5,6,7,10,11,12,

Device Mode

The choice: Standard Parallel Port Mode, EPP Mode, ECP Mode, EPP Mode & ECP Mode.

3.2.9 Sandybridge PPM Configuration



EIST

Enable/Disable Intel SpeedStep.

CPU C3 Report

Enable/Disable CPU C3(ACPI C2) report to OS.

CPU C6 Report

Enable/Disable CPU C6(ACPI C3) report to OS.

CPU C7 Report

Enable/Disable CPU C7(ACPI C3) report to OS.

Long duration power limit

Long duration power limit in Watts, 0 means use factory default.

Long duration maintained

Time window which the long duration power is maintained.

Short duration power limit

Short duration power limit in Watts, 0 means use factory default.

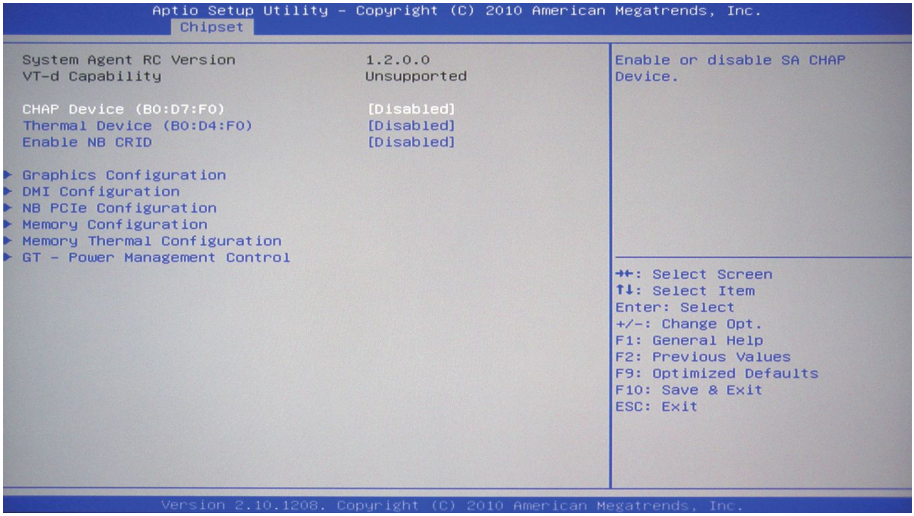
TCC active offset

Offset from the factory TCC activation temperature.

3.3 Chipset

This section allows you to configure and improve your system; also, set up some system features according to your preference.

3.3.1 System Agent (SA) Configuration



CHAP Device (B0:D7:F0)

Enable or disable SA CHAP Device.

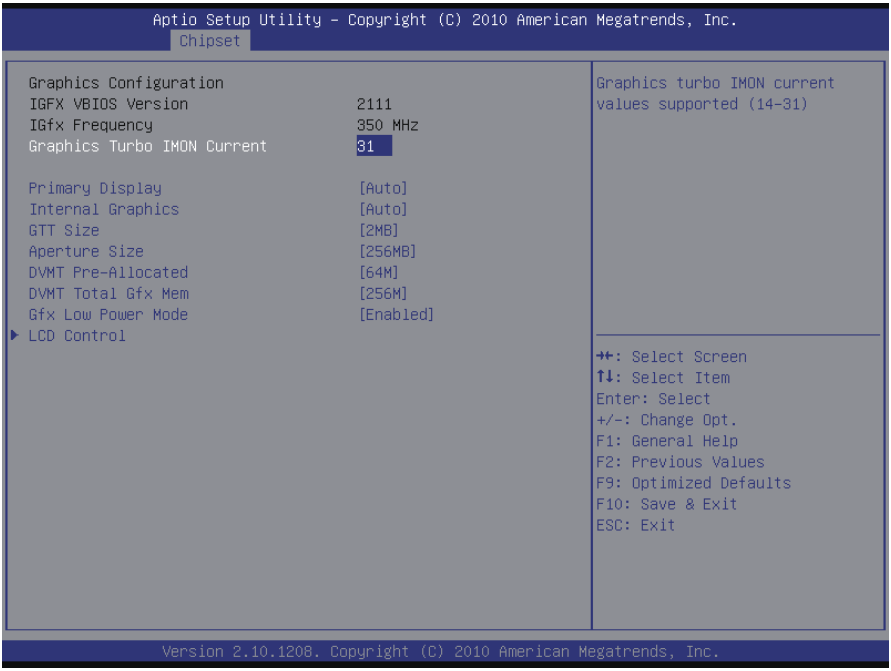
Thermal Device (B0:D4 F0)

Enable or disable SA Thermal Device.

Enable NB CRID

Enable or disable NB CRID WorkAround.

Graphics Configuration



Primary Display

Select which of IGFX/PEG/PCI Graphics Devices should be Primary Display or select SG for Switchable Gfx.

Internal Graphics

Keep IGD enabled based on the option.

GTT Size

Select the GTT Size: 1MB, 2MB.

Aperture Size

Select the Aperture Size: 128MB, 256MB, 512MB.

DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device: 0M~512M.

DVMT Total Gfx Mem

Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device: 128M, 256M, MAX.

Gfx Low Power Mode

This option is applicable for SFF only.

LCD Control

Primary IGFX Boot Display

Select the Video Device which will be activated during POST. This has no effect if external graphics present.
Secondary boot display selection will appear based on your selection.
VGA modes will be supported only on primary display.

LCD Panel Type

Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item: VBIOS Default, 640x480 LVDS ~ 2048x1536 LVDS.

Panel Scaling

Select the LCD panel scaling option used by the Internal Graphics Device: Auto, Off, Force Scaling.

Backlight Control

The choice: PWM Inverted (Default), PWM Normal, GMBus Inverted and GMBus Normal.

BIA

The choice: VBIOS Default, Disabled and Level 1/2/3/4/5.

Spread Spectrum clock Chip

The default setting is Off. Other options are:
Hardware: Spread is controlled by chip.
Software: Spread is controlled by BIOS.

Active LFP

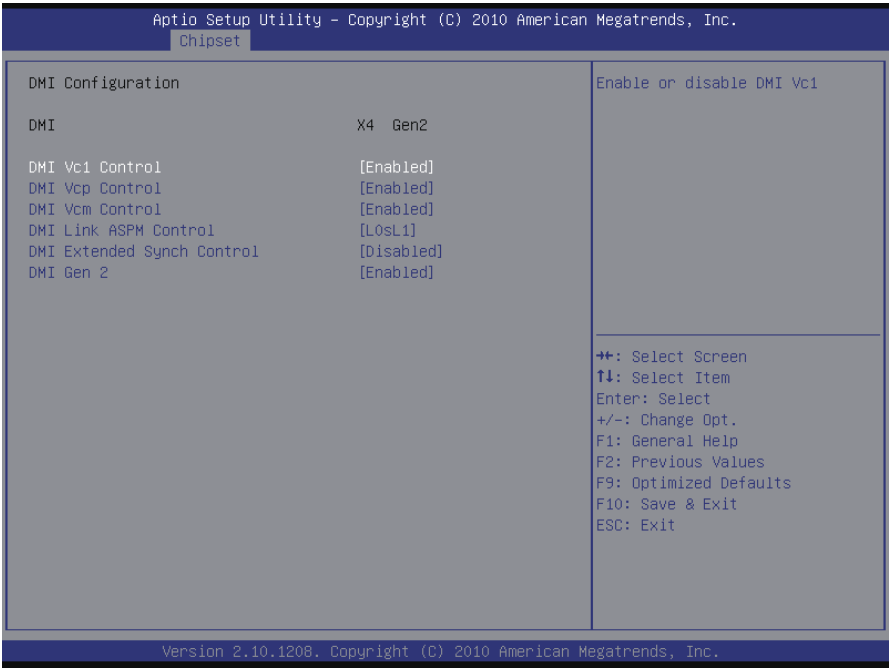
Select the Active LFP Configuration.
No LVDS: VBIOS does not enable LVDS.
Int-LVDS: VBIOS enables LVDS driver by Integrated encoder.
SDVO LVDS: VBIOS enables LVDS driver by SDVO encoder.
eDP Port-A: LFP driven by Int-DisplayPort encoder from Port-A.

Panel Color Depth

Select the LFP panel color depth: 18 Bit, 24 Bit.

DMI Configuration

Control various DMI functions.



DMI Vc1/Vcp/Vcm Control

Enable or disable DMI Vc1/Vcp/Vcm.

DMI Link ASPM Control

Enable or disable the control of Active State Power Management on SA side of the DMI Link.
The choice: Disabled, L0s, L1, L0sL1

DMI Extended Synch Control

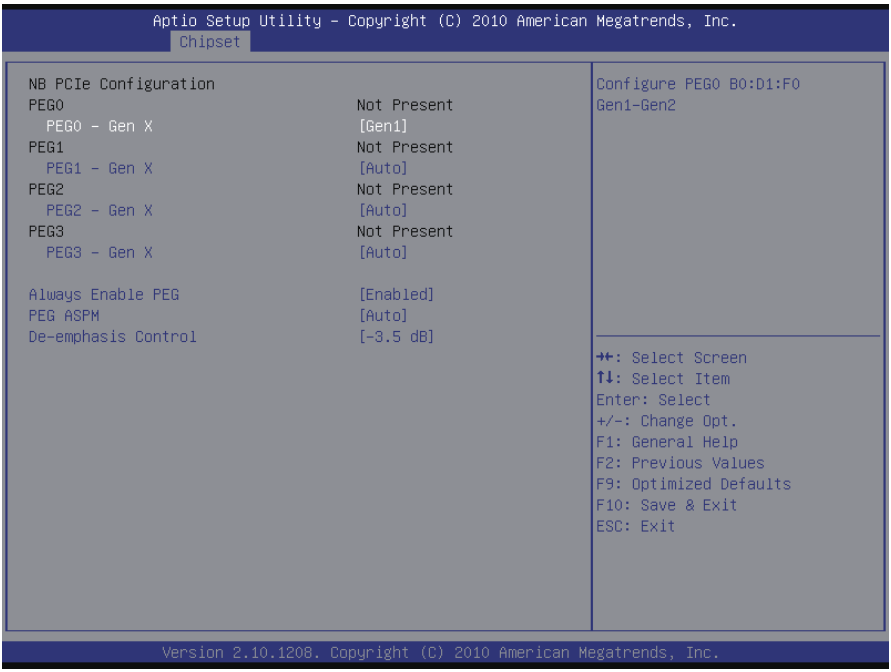
Enable or disable DMI Extended Synchronization.

DMI Gen 2

Enable or disable DMI Gen 2.

NB PCIe Configuration

Configure NB PCIe Express Settings.



PEG0 – Gen X

Configure PEG0 B0:D1:F0 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

PEG1 – Gen X

Configure PEG1 B0:D1:F1 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

PEG2 – Gen X

Configure PEG2 B0:D1:F2 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

PEG3 – Gen X

Configure PEG3 B0:D6:F0 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

Always Enable PEG

Enable the PEG slot.

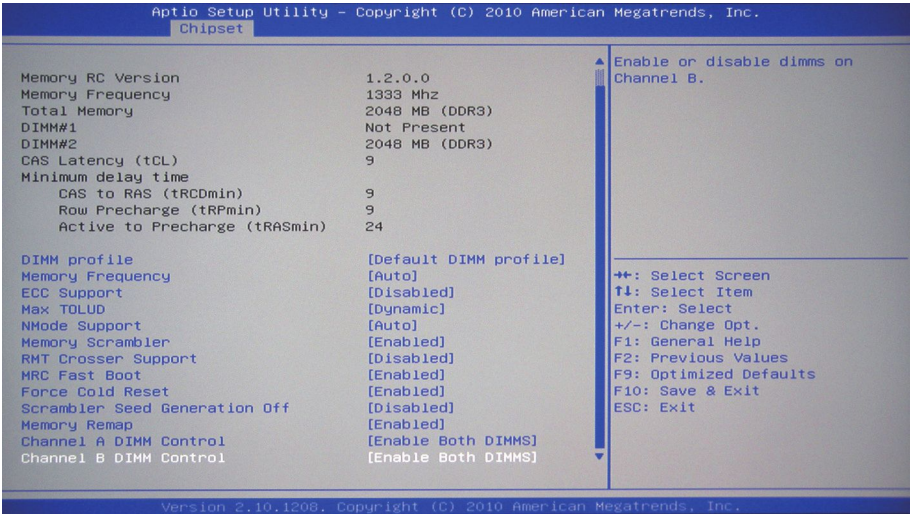
PEG ASPM

Control ASPM support for the PEG Device. This has no effect if PEG is not the currently active device.
The choice: Disabled, Auto, ASPM L0s, ASPM L1, ASPM L0sL1

De-emphasis Control

Configure the De-emphasis control on PEG.
The choice: -6 dB, -3.5 dB

Memory Configuration



DIMM profile

Select DIMM timing profile that should be used.
The choice: Default DIMM profile, XMP profile 1, XMP profile 2

Memory Frequency

Maximum Memory Frequency Selections in Mhz.
The choice: Auto, 1067, 1333, 1600, 1867, 2133

ECC Support

Enable or disable DDR Ecc Support.

Max TOLUD

Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.
The choice: Dynamic, 1GB, 1.25 GB, 1.5 GB, 1.75 GB, 2GB, 2.25 GB, 2.5 GB, 2.75 GB, 3 GB, 3.25 GB

NMode Support

NMode Support Option.
The choice: Auto, 1 N Mode, 2 N Mode

Memory Scrambler

Enable or disable Memory Scrambler support.

RMT Crosser Support

Enable or disable RmtCrosserEnable support.

MRC Fast Boot

Enable or disable MRC fast boot.

Force Cold Reset

Force cold reset or choose MRC cold reset mode, when cold boot is required during MRC execution.
NOTE: If ME 5.0MB is present, Force cold reset is required!

Scrambler Seed Generation Off

Control Memory Scrambler Seed Generation.
Enable - do not generate scrambler seed.
Disable - generate scrambler seed always.

Memory Remap

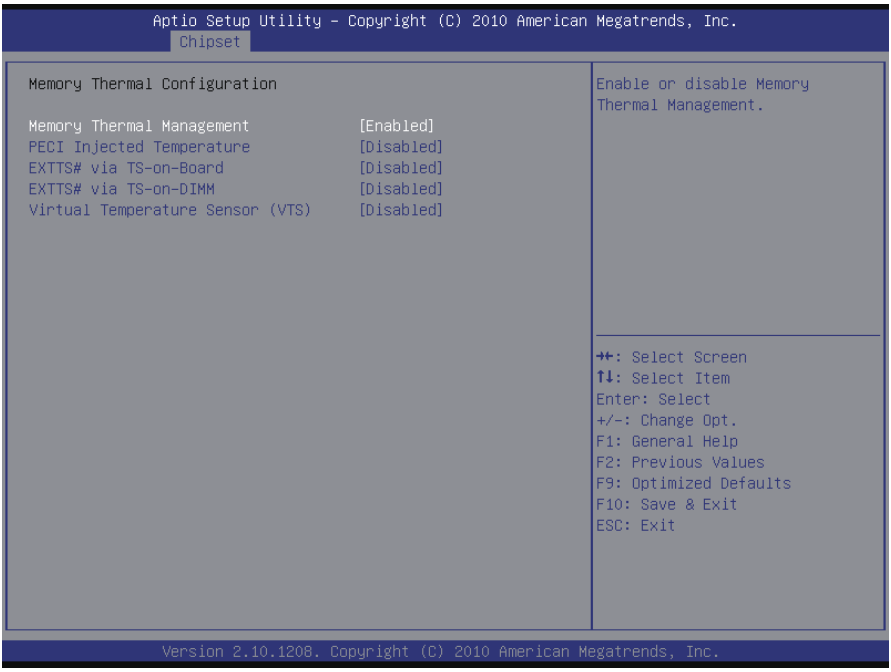
Enable or disable memory remap above 4G.

Channel A DIMM Control

Enable or disable dimms on channel A.

Memory Thermal Configuration

Memory Thermal Configuration Options.



Memory Thermal Management

Enable or disable Memory Thermal Management.

PECI Injected Temperature

Enable or disable memory temperatures to be injected to the processor via PECI.

EXTT# via TS-on-Board

Enable or disable routing TS-on-Board's ALERT# and THERM# to EXTTS# pins on the PCH.

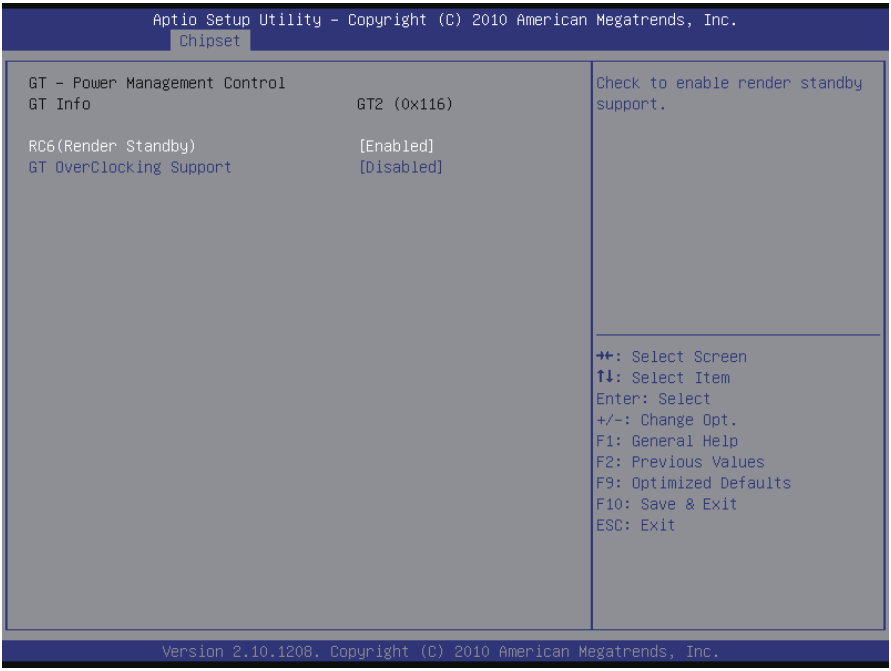
EXTT# via TS-on-DIMM

Enable or disable routing TS-on-DIMM's ALERT# to EXTTS# pin on the PCH.

Virtual Temperature Sensor (VTS)

Enable or disable Virtual Temperature Sensor.

GT – Power Management Control



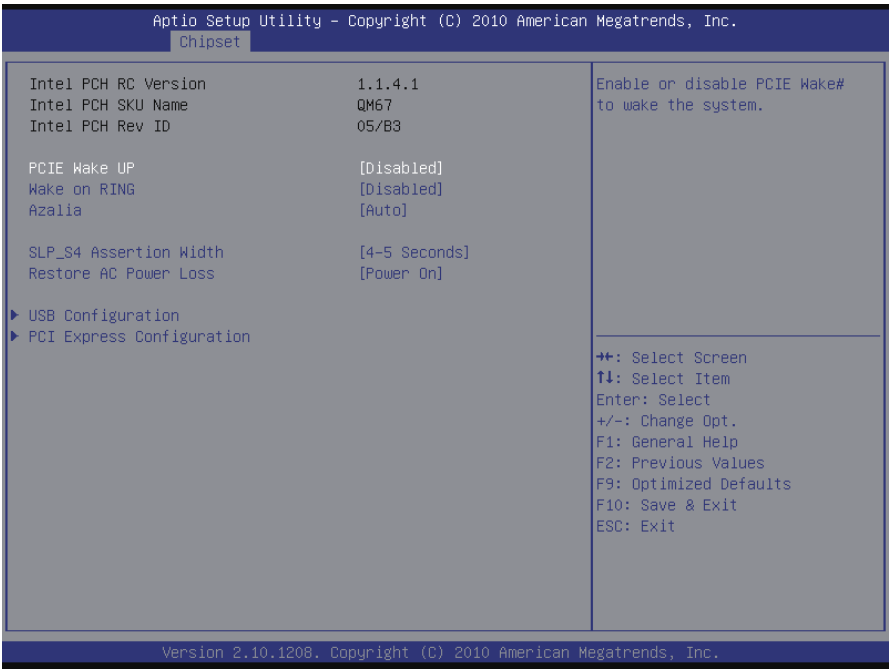
RC6 (Render Standby)

Check to enable render standby support.

GT Overclocking Support

Enable or disable GT Overclocking Support.

3.3.2 PCH-IO Configuration



PCIE Wake UP

Enable or disable PCIE Wake# to wake the system.

Wake on RING

Enable or disable Wake on RING (WOR). Computer will start up simply by applying power to a connected external modem if WOR is enabled.

Azalia

Control detection of the Azalia device.
Disabled = Azalia will be unconditionally disabled.
Enabled = Azalia will be unconditionally enabled.
Auto = Azalia will be enabled if present, disabled otherwise.

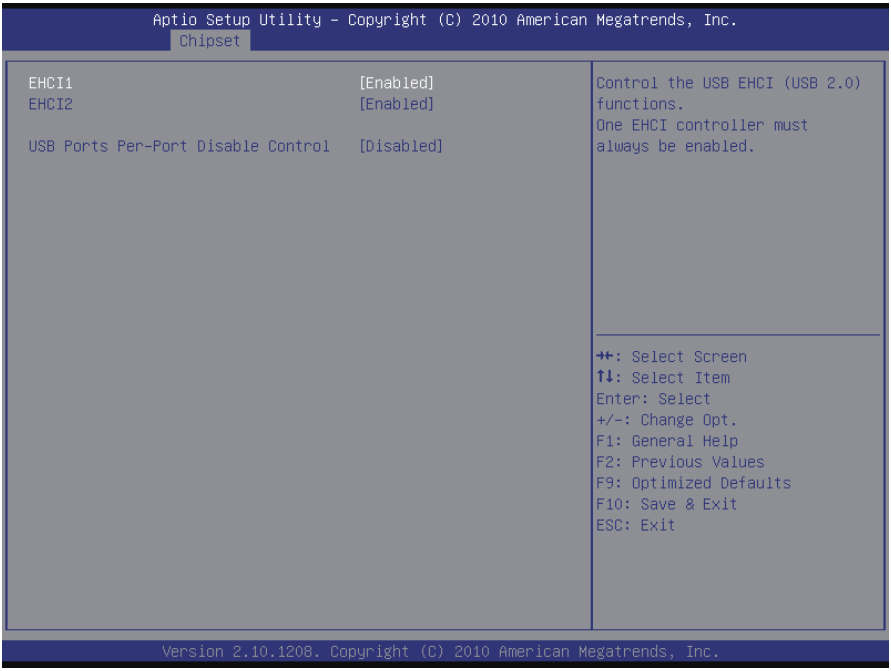
SLP_S4 Assertion Width

Select a minimum assertion width of the SLP_S4# signal.
The choice: 1-2 Seconds, 2-3 Seconds, 3-4 Seconds, 4-5 Seconds

Restore AC Power Loss

Select AC power state when power is re-applied after a power failure.

USB Configuration



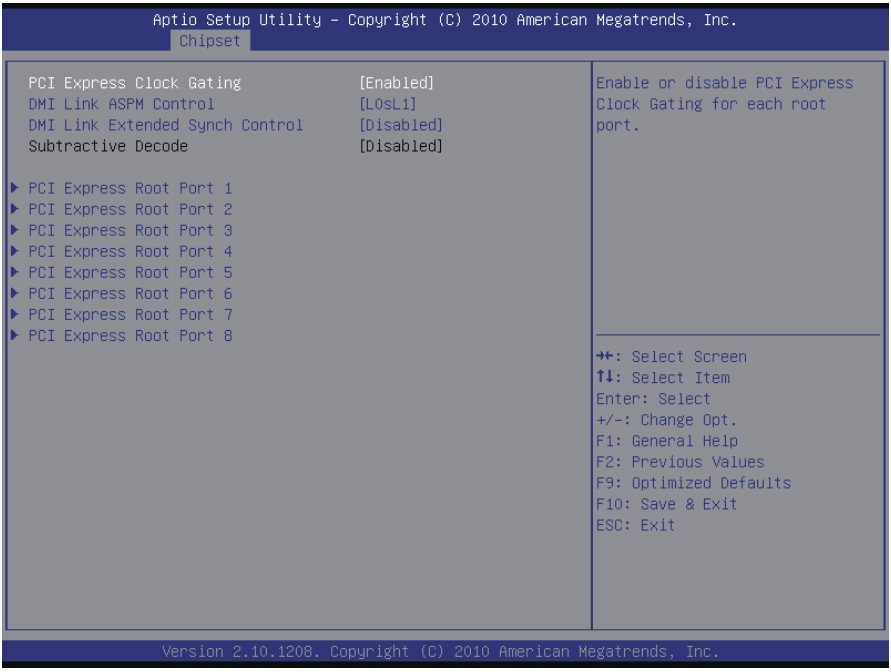
EHCI1~2

Control the USB EHCI (USB2.0) functions.
One EHCI controller must always be enabled.

USB Ports Per-Port Disable Control

Enable or disable each of the USB ports (0~9).

PCI Express Configuration



PCI Express Clock Gating

Enable or disable PCI Express Clock Gating for each root port.

DMI Link ASPM Control

The control of Active State Power Management on both NB side and SB side of the DMI Link.

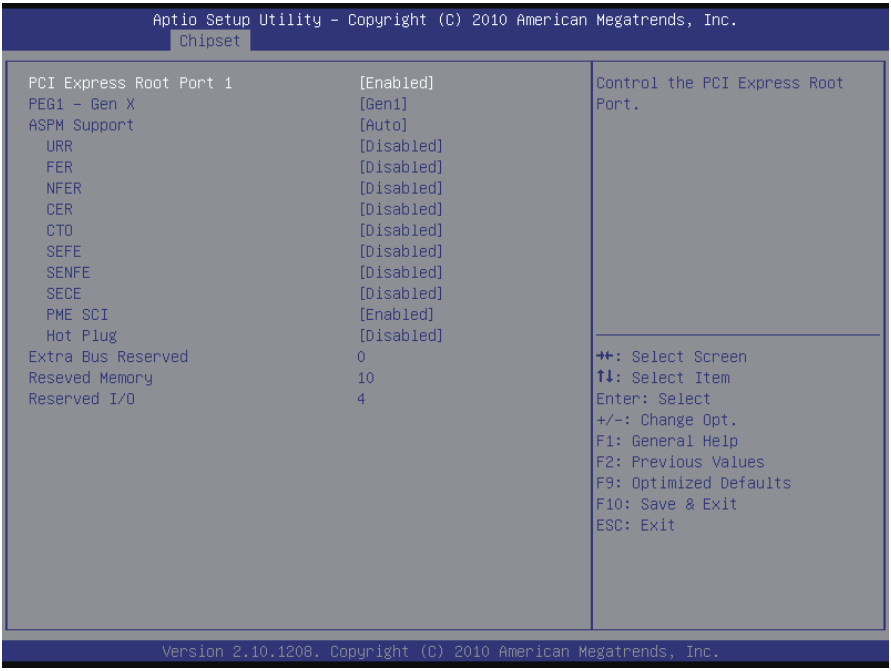
DMI Link Extended Synch Control

The control of Extended Synch on SB side of the DMI Link.

Subtractive Decode

Enable or disable Subtractive Decode.

PCI Express Root Port 1~8



PCI Express Root Port 1~8

Control the PCI Express Root Port.

PEG1 – Gen X

Configure PEG1 B0 :D1 :F1 Gen1-Gen2
The choice: Auto, Gen1, Gen2

ASPM Support

Set the ASPM Level to Disabled, L0s, L1, L0sL1, Auto
Force L0 - Force all links to L0 State
AUTO - BIOS auto configuration
DISABLE - Disable ASPM

URR

Enable or disable PCI Express Unsupported Request Reporting.

FER

Enable or disable PCI Express Device Fatal Error Reporting.

NFER

Enable or disable PCI Express Device Non-Fatal Error Reporting.

CER

Enable or disable PCI Express Device Correctable Error Reporting.

CTO

Enable or disable PCI Express Completion Timer TO.

SEFE

Enable or disable Root PCI Express System Error on Fatal Error.

SENFE

Enable or disable Root PCI Express System Error on Non-Fatal Error.

SECE

Enable or disable Root PCI Express System Error on Correctable Error.

PME SCI

Enable or disable PCI Express PME SCI.

Hot Plug

Enable or disable PCI Express Hot Plug.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

Reserved Memory

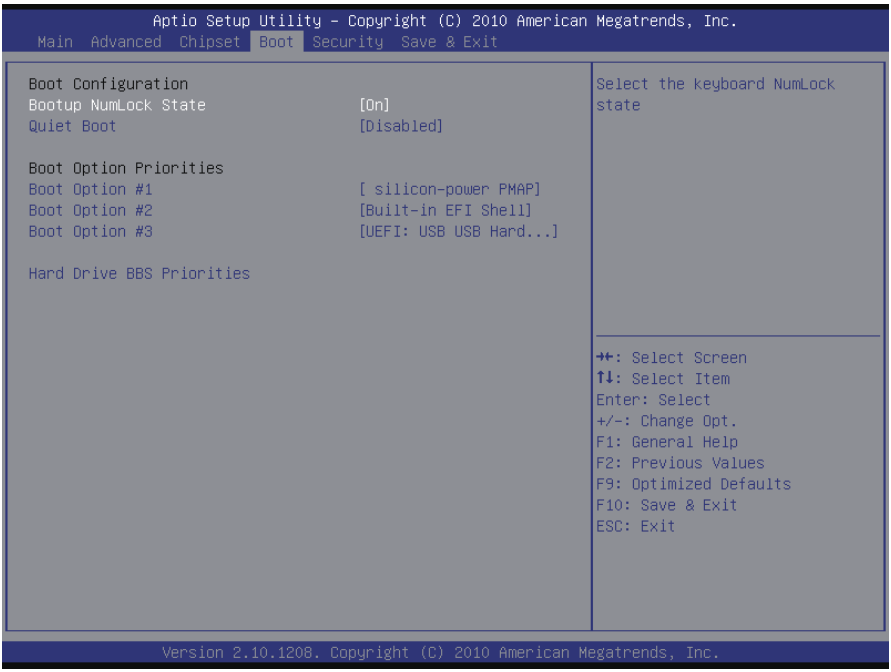
Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserved I/O

Reserved I/O (4k/8k/12k/16k/20k) Range for this Root Bridge.

3.4 Boot Settings

The Boot menu items allow you to change the system boot options.



Boot Configuration

Bootup NumLock State

This setting determines whether the Num Lock key should be activated at boot up.

Quiet Boot

This allows you to select the screen display when the system boots.

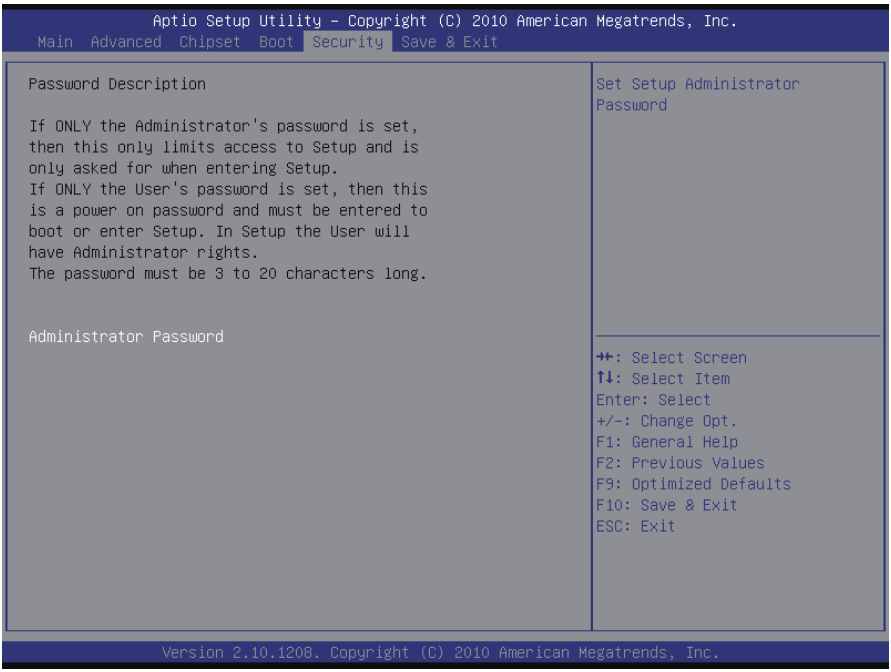
Boot Option Priorities

Select the boot sequence of the hard drives.

Hard Drive BBS Priorities

This allows you to set the hard drive boot priority. The BIOS will attempt to arrange the hard disk boot sequence automatically. You can also change the booting sequence. The number of device items that appears on the screen depends on the number of devices installed in the system.

3.5 Security



Administrator Password

Use the Administrator Password to set or change a administrator password.

ENTER PASSWORD

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <ESC> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED

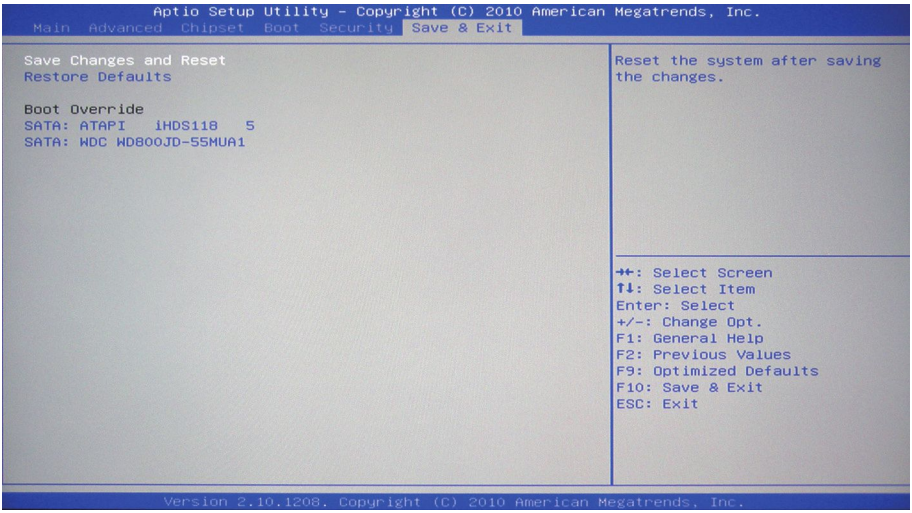
When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from

changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You can determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If it’s set to “Setup”, prompting only occurs when trying to enter Setup.

3.6 Save & Exit



Save Changes and Reset

Pressing <Enter> on this item and it asks for confirmation:

Save configuration changes and exit setup?

Pressing <OK> stores the selection made in the menus in CMOS - a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

Restore Defaults

Restore system to factory default.
Pressing <Enter> on this item and it asks for confirmation prior to executing this command.

Boot Override

This group of functions includes a list of tokens, each of them corresponding to one device within the boot order. Select a drive to immediately boot that device regardless of the current boot order.

3.7 AMI BIOS Checkpoints

3.7.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

3.7.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed

0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.

0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available

0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)

0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable

0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found

0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

Appendix

Appendix A: I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
0x00000000-0x00000CF7	PCI bus
0x00000000-0x00000CF7	Direct memory access controller
0x00000D00-0x0000FFFF	PCI bus
0x0000F000-0x0000F03F	Video Controller (VGA Compatible)
0x0000F060-0x0000F07F	Ethernet Controller
0x00000A79-0x00000A79	ISAPNP Read Data Port
0x00000279-0x00000279	ISAPNP Read Data Port
0x00000274-0x00000277	ISAPNP Read Data Port
0x00000081-0x00000091	Direct memory access controller
0x00000093-0x0000009F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller

0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x000004D0-0x000004D1	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000070-0x00000070	System CMOS/real time clock
0x00000080-0x00000080	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x00001000-0x0000100F	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x00000400-0x00000453	Motherboard resources
0x00000458-0x0000047F	Motherboard resources
0x00000500-0x0000057F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x00000454-0x00000457	Motherboard resources
0x00000A00-0x00000A1F	Motherboard resources
0x00000290-0x0000029F	Motherboard resources
0x00000060-0x00000060	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard

0x00000064-0x00000064	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00000378-0x0000037F	Printer Port (LPT1)
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000044-0x0000005F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x000000F0-0x000000FF	Numeric data processor
0x0000F130-0x0000F137	Standard Dual Channel PCI IDE Controller
0x0000F120-0x0000F123	Standard Dual Channel PCI IDE Controller
0x0000F110-0x0000F117	Standard Dual Channel PCI IDE Controller
0x0000F100-0x0000F103	Standard Dual Channel PCI IDE Controller
0x0000F0F0-0x0000F0FF	Standard Dual Channel PCI IDE Controller
0x0000F0E0-0x0000F0EF	Standard Dual Channel PCI IDE Controller
0x0000F040-0x0000F05F	SM Bus Controller
0x0000F0D0-0x0000F0D7	Standard Dual Channel PCI IDE Controller
0x0000F0C0-0x0000F0C3	Standard Dual Channel PCI IDE Controller
0x0000F0B0-0x0000F0B7	Standard Dual Channel PCI IDE Controller
0x0000F0A0-0x0000F0A3	Standard Dual Channel PCI IDE Controller
0x0000F090-0x0000F09F	Standard Dual Channel PCI IDE Controller
0x0000F080-0x0000F08F	Standard Dual Channel PCI IDE Controller
0x000003B0-0x000003BB	VgaSave
0x000003C0-0x000003DF	VgaSave

0x000001CE-0x000001CF	VgaSave
0x000002E8-0x000002EF	VgaSave

Appendix B: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 9	Microsoft ACPI-Compliant System
IRQ 16	PCI standard PCI-to-PCI bridge
IRQ 16	Standard Enhanced PCI to USB Host Controller
IRQ 16	PCI standard PCI-to-PCI bridge
IRQ 11	Video Controller (VGA Compatible)
IRQ 11	PCI PCI Simple Communications Controller
IRQ 5	Ethernet Controller
IRQ 5	SM Bus Controller
IRQ 22	Microsoft UAA Bus Driver for High Definition Audio
IRQ 23	Standard Enhanced PCI to USB Host Controller
IRQ 8	System CMOS/real time clock
IRQ 0	System timer
IRQ 1	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
IRQ 12	Microsoft PS/2 Mouse
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 13	Numeric data processor
IRQ 19	Standard Dual Channel PCI IDE Controller
IRQ 19	Standard Dual Channel PCI IDE Controller

Appendix C: BIOS Memory Map

Address	Device Description
0xA0000-0xBFFFF	PCI bus
0xA0000-0xBFFFF	VgaSave
0xD0000-0xD3FFF	PCI bus
0xD4000-0xD7FFF	PCI bus
0xD8000-0xDBFFF	PCI bus
0xDC000-0xDFFFF	PCI bus
0xE0000-0xE3FFF	PCI bus
0xE4000-0xE7FFF	PCI bus
0x7DA00000-0xFEAFFFFF	PCI bus
0x7DA00000-0xFEAFFFFF	Motherboard resources
0xF7800000-0xF7BFFFFF	Video Controller (VGA Compatible)
0xE0000000-0xEFFFFFFF	Video Controller (VGA Compatible)
0xF7C2B000-0xF7C2B00F	PCI Simple Communications Controller
0xF7C00000-0xF7C1FFFF	Ethernet Ethernet Controller
0xF7C28000-0xF7C28FFF	Ethernet Ethernet Controller
0xF7C27000-0xF7C273FF	Standard Enhanced PCI to USB Host Controller
0xF7C20000-0xF7C23FFF	Microsoft UAA Bus Driver for High Definition Audio
0xF7C26000-0xF7C263FF	Standard Enhanced PCI to USB Host Controller
0xFF000000-0xFFFFFFFF	Intel(R) 82802 Firmware Hub Device
0xFF000000-0xFFFFFFFF	Motherboard resources
0xFED00000-0xFED003FF	High Precision Event Timer, HPET
0xF7C25000-0xF7C250FF	SM Bus Controller
0xFED40000-0xFED44FFF	System board
0xFED1C000-0xFED1FFFF	Motherboard resources
0xFED10000-0xFED17FFF	Motherboard resources
0xFED18000-0xFED18FFF	Motherboard resources

0xFED19000-0xFED19FFF	Motherboard resources
0xF8000000-0xFBFFFFFF	Motherboard resources
0xFED20000-0xFED3FFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEEFFFFF	Motherboard resources
0x20000000-0x201FFFFF	System board
0x40000000-0x401FFFFF	System board

Appendix D: Digital I/O Setting

Below are the source codes written in C, please take them for Digital I/O application examples. The default I/O address is 6Eh.

C language Code

```
/*                                                              */
/*          SMBus Device Register Reader  program by Rex Chin. */
/*                                                              */
/*-----     Include Header Area -----*/
#include “math.h”
#include “stdio.h”
#include “dos.h”

/*-----     routing, sub-routing -----*/
void main(int argc, char *argv[])
{
          int SMB_PORT_AD  = 0x580;
          int SMB_DEVICE_ADD = 0x6e;       /*75111R’s Add=6eh */
          int i,j;

          printf(“ Fintek F75111 DIO LED TEST Program Ver:0.1 \n”);
          printf(“ Warning: This tools is test only. \n”);

/*        Index 10, GPIO1x Output pin control          */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x10,0xff);
          delay(10);

          printf(“All Digital I/O LED ON ...   \n”);
/*        Index 11, GPIO1x Output Data value           */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0x00);

          delay(3000);

          printf(“All Digital I/O LED OFF ...  \n”);
/*        Index 11, GPIO1x Output Data value           */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0xff);

          delay(3000);

          printf(“Digital I/O pin 7,5,3,1 LED OFF ...\n”);
/*        Index 11, GPIO1x Output Data value           */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0xAA);
```

```
            delay(3000);
            printf("Digital I/O pin 6,4,2,0 LED OFF ...\n");
/*          Index 11, GPIO1x Output Data value              */
            SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0x55);
            delay(1500);

}

SMB_Byte_READ(int SMPORT, int DeviceID, int REG_INDEX)
{
            outportb(SMPORT+02, 0x00);          /* clear */
            outportb(SMPORT+00, 0xff);          /* clear */
            delay(10);
            outportb(SMPORT+04, DeviceID+1);        /* clear */
            outportb(SMPORT+03, REG_INDEX);           /* clear */
            outportb(SMPORT+02, 0x48);          /* read_byte */
            delay(10);
            printf(" %02x ",inportb(SMPORT+05));
}

SMB_Byte_WRITE(int SMPORT, int DeviceID, int REG_INDEX, int REG_DATA)
{
            outportb(SMPORT+02, 0x00);          /* clear */
            outportb(SMPORT+00, 0xff);          /* clear */
            delay(10);
            outportb(SMPORT+04, DeviceID);              /* clear */
            outportb(SMPORT+03, REG_INDEX);           /* clear */
            outportb(SMPORT+05, REG_DATA);            /* read_byte */
            outportb(SMPORT+02, 0x48);          /* read_byte */
/*          delay(10);
            printf(" %02x ",inportb(SMPORT+05)); */
}
```